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RC 4320 MAGNETIC DRUM STORE CONTROLLER.

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RCSL: 51-VB769

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RC 4320 MAGNETIC DRUM STORE

Technical Manual

for

Drum Controller, DRC 401

A/S REGNECENTRALEN

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2000 Copenhagen F

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1. SPECIFICATIONS.

Capacity	65,536 words expandable in modules of 65,536 words up to 524,288 words.
Transfer Rate	50,000 words/sec.
Word Size	24 bits
Segment Size	256 words
Block Size	Variable numbers of segments.
Mean Access Time	10.5 msec.
Transfer Time	5.2 msec./segment
Mean Time for Access and Transfer of a block containing n Segments	$(10.5 + n \times 5.2)$ msec.
Reliability	Drum bearing life exceeds 100,000 hours of operation. Mean time between failures is 15,000 hours.
Power Supply	220 V ± 10 per cent, 50 Hz ± 4 per cent max. line current 6A operating current 1A
Power Dissipation	120 kcal/hour inside the drum can.
Temperature Range	10 degrees C to 50 degrees C surface temperature of can.
Drum Size	Width: 483 cm (19 inches) Depth: 580 cm Height: 650 cm
Controller Size	One 3-row unit mounted in the controller cabinet.

2. LOGICAL STRUCTURE.

This chapter describes the logical structure of RC 4320 Magnetic Drum Store used in connection with the RC 4000 Computer.

2.1. Main Characteristics.

The minimum drum capacity is 64K words of 24 bits each. The capacity can be extended in modules of 64K words up to a maximum of 512K words. The drum is divided into segments of 256 words each. It can transfer a data block consisting of a variable number of segments directly to or from the internal store. The average block transfer time in milliseconds is:

$$10.5 + 5.2 \times \text{number of segments}$$

The drum operates on the high-speed data channel, but uses the low-speed data channel to transfer commands and control parameters to or from the working registers. Protection keys are not stored in the drum.

2.2. Commands.

The drum controller accepts sense and control commands, the latter with four modifications.

In the input/output instruction specifying the sense command, the value of the modifier field, i.e. bits 18-21 in the effective address, is irrelevant.

The use of read commands, write commands, and other modifications of the control command than specified has no effect at all.

2.3. Control Commands.

The following control commands are available:

5	transfer first	<first segment>
9	transfer size	<number of segments>
13	input	<first storage address>
17	output	<first storage address>

The integers denote the values of bits 18-23 in the effective address of the input/output instruction. The parameters in the brackets AND denote the contents of the working register selected by the input/output instruction.

The parameters first segment, number of segments, and first storage address are interpreted modulo 2048, 512, and 262 144, respectively. The rightmost bit in the parameter, first storage address, is ignored. Thus it is irrelevant whether the parameter refers to the left or the right half of the storage word.

2.4. Input and Output.

The input or output of a block requires three control commands.

Two transfer commands are used to define the first segment and the number of segments on the drum.

One input or output command initiates the transfer defining the first address of the storage buffer.

After the initiation of input or output, the drum is busy until the operation is either completed successfully or terminated by an error condition. The drum delivers an interrupt signal when it becomes available.

2.5. Sense Command.

When the drum is available, a status word can be transferred to a working register by means of a sense command.

The status bits have the following meaning:

status bit 0:	(not used = 0)
status bit 1:	parity error
status bit 2:	synchronization error
status bit 3:	data overrun
status bit 4-23:	(not used = 0)

Parity_error indicates a parity error in one or more data words during the transfer.

Synchronization_error indicates a parity error on the block track of the drum. This is a serious hardware malfunction.

Data_overrun indicates overloading of the high-speed data channel due to which the block transfer immediately has been stopped.

3. HARDWARE STRUCTURE.

This chapter describes the hardware structure of the RC 4320 Magnetic Drum Store consisting of the drum VRC 1016 and the controller DRC 401. See fig. 1.

3.1. Mechanical Construction.

The drum is a Vermont Research Corporation type 1016 rotating memory drum with flying heads. The recording heads are mounted in head pads, each pad containing 16 active data heads. At running speed, the head pads fly on a hydrodynamic air bearing formed by the laminar film of air close to the rotating drum surface. The head pads are supported in groups of four on the head bars. Thus a head bar contains 64 data heads. Up to eight head bars can be mounted on the drum giving a maximum of 512 heads. This is equivalent to 512 tracks each containing four segments of 256 data words of 24 bits.

Segment addressing (see DRC 023, 021, 007, 035, 036) is carried out in this way:

- | | |
|-----------|--|
| bit 13 | specifies first second group selection circuits. |
| bit 14-15 | specifies the selected head bar in the group. |
| bit 16-17 | specifies the selected head pad in the head bar. |
| bit 18-21 | specifies the selected data head in the head pad. |
| bit 22-23 | specifies the selected sector on the track, and therefore they are not supplied to the drum. |

The selection diodes, address lines and head pad selection circuits, are mechanical situated on the head bars inside the drum can, but the rest of selection as well as the reading and writing amplifiers are situated in an 11-position card frame with the drum base plate.

The drum and the drum controller are connected via one multicable (see DRC 006, 023, 004) containing all signals to and from the drum and also the d.c. supply voltages to the drum electronic. The 220V a.c. for the drum is supplied directly from POW406 via another cable, see fig. 1.

The Drum Controller DRC 401 is a 3-row sub-frame placed in the I/O controller cabinet, and connected to the low-speed bus and the high-speed bus.

3.2. Register Structure.

The drum controller registers can be divided into four groups, Data Registers, Drum Address Registers, Core Store Address Registers, and Control Registers. See fig. 2.

Data Registers:

- WB(0:23) Word Buffer. Connected to the high-speed bus for parallel transport of 24-bit words between core store and register SP.
- SP(0:23) Serial Parallel. Transfers the 24-bit words to serial during write operation, and converts the incoming data bits from serial to parallel during read operation.
- PW(0:23) Parity Word. Twenty-four one-bit registers used to generate the parity word.

This data registers are implemented on 12 circuit cards, each containing 2 bits of the registers and two comparator circuits for comparing bit n and n+1 of WB and PW.

The data registers are shown on DRC 018, 019, 020 and the controlling and timing circuits on DRC 016, 017. The contents of the registers are given in the timing diagrams fig. 4 and 5.

Drum Address Registers:

- DSA(12:23) Drum Store Address. When a block transport starts, it contains the address of the first segment that has to be transferred (see DRC 007, 035, 036). As long as NBS(15:23) is different from 0, the register is counted one up for each transferred segment.
- DTA(0:8) Drum Track Address. This register controls directly the address lines to the drum, see DRC 021, 023). The contents is a copy of the contents of DSA(12:21) brought up to date in every sector gap.

Core Store Address Registers:

CSA(5:22) Core Store Address. When a block transport starts, it contains the address of the first word that has to be transferred, see DRC 009, 010, 035, 036. The register is counted one up for each transferred word, see DRC 013.

Control Registers:

NBS(15:23) Number of Segments. When a block transport starts, it contains the number of segments that has to be transferred in the block transport, see DRC 008, 035, 036. The register is counted one down for each transferred segment, see DRC 013.

Bit(0:4) Bit Address Register. See DRC 015, 013, 012. A modulo 24 counter controlled by the clock pulse. It will shift every 800 nanoseconds.

Word(0:8) Word Address Register. See DRC 014, 013, 012. A modulo 268 counter controlled by the clock pulse. It will shift every time Bit(0:4) goes from 23 to 0.

Sector(0:1) Sector Address Register. See DRC 015, 013, 012. A modulo 4 counter controlled by the clock pulse. It will shift every time (Word(0:8), Bit(0:4)) goes from (257,3) to (257,4).

Time 000t150
Time 200t350
Time 400t550
Time 600t750

Timing Registers controlled by the clock pulse from the drum, see DRC 006. The Sector(0:1)conWord(0:8)conBit(0:4) register always indicates the rotational position of the drum. The register value is reset to (0,257,4) when the drum index pulse occurs, see fig. 3. When this has been done once, when the system was started, then this resetting should be unnecessary, because the 25728 clock pulses will automatically hold the register correctly synchronized with the drum. If this unnecessary synchronization occurs at array, other times than (3,257,3), or does not occur at all, this is detected as a synchronization error, see DRC 021.

Status(0:23)

Status Register. See fig. 2. This register stores different types of errors that may occur from the moment a block transfer is initiated, see DRC 005. The status word can be transferred to the core store when the drum is ready by means of a sense command.

Status(1) indicates a parity error.

Status(2) indicates a synchronization error, or a too low drum speed, or prospectively an address error. (Address errors are only detected during input operations).

Status(3) indicates data overrun on the high-speed bus.

(This may happen if so many high-speed devices operate simultaneously that a CYS Request from the drum is not answered within 18 microseconds. See fig. 6. Status(0) and Status(4:23) are 0.

3.3. Data Format.

On the drum the data are cyclically stored bit by bit, see fig. 4 and 5. The format of the data words is given in fig. 6. It is shown how half of the data bits are inverted during the transfer from high-speed bus to word buffer, WB(0:23), and how the same bits later on, when the recorded word has been read, are transferred from WB to the high-speed bus with their negated values. The reason for this is to increase the efficiency of the parity control system. On one track there are 4 sectors, each containing 256 data words and 12 other words giving a total of $4 \times 268 \times 24 = 25728$ bits. Identification of a certain bit is carried out by means of register Sector(0:1)conWord(0:8)conBit(0:4). If a track switching is necessary for getting access to a segment, this track switching takes place between bit 3 and bit 4 in word 257. This is the beginning of the sector. Hereafter follows a Write/Read switching time equivalent to about four words. The following words are different from 0, and are used to synchronize the self-clocking peak detector. During reading operation, this preamble words which actually give the segment address are checked. Address checking takes place for word 267. The following words, numbered 0 to 255, contain the 256 data words, logically regarded as one segment. Hereafter follows word 256 containing the parity word. Then finally four bits of word 257 belong to the sector, but are not used for information.

3.4. Test Performance.

6 different types of functional controls and data checkings are carried out. The test results may be examined by means of a sense command, giving a 3-bit extract of the controller status. More detailed, the following are tested:

Speed Control (DRC 004) (Fig. 9,10)	The frequency of the main clock is detected, and, if it is above 95 per cent of normal frequency, the Drum Speed is OK. Otherwise, Status(2) will be set to logical 1. If an input/output operation is running, it will be stopped immediately.
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Power Control (DRC 004)	All d.c. power supplies to the drum electronic as well as to the controller are controlled. If they are above approximately 90 per cent of nominal value, the DRC Power is OK. If not, no writing on the drum can be done, and the device will be disconnected.
----------------------------	---

When the two abovementioned signals are logically 1, a green lamp on the operator control panel will switch on, indicating that device N (N is the wired-in device number of RC 4320) should be capable of handling data transports, see DRC 001.

Synchronization Control (DRC 021) (Fig. 3)	The controller counts the clock pulses from the drum. There must be exactly 25728 Read Strokes equally spread around the Clock Track. If not, Status(2) is set to logical 1.
--	--

Address Control (DRC 005) (Fig. 4)	In the head of every segment, the segment address is written. During Read operation, this number is compared with the address of the segment to be read. They must be equal, otherwise Status(2) is set to logical 1 and no data transport will be carried out.
--	---

Parity Control
(DRC 005)
(Fig. 5)

During writing a segment, a 24-bit parity word is generated. Bit n is the Boolean sum modulo 2 of all 1-bits in position n for the 256 data words and the segment address word. (Please notice that the data words are formed by the information on the high-speed bus by inverting some of the bits, see fig.6). The parity word is written immediately following the last data word. During reading, a parity word is generated in the same way, but now the data words are the readed words. Then this parity word is compared with the readed parity word. They have to be identical. Otherwise Status(1) is set to logical 1.

BUS Control
(DRC 005)
(Fig. 6)

Overloading of the high-speed bus will result in a too late response from the Core Store Controller upon Cycle Requests from the device. If this happens, Status(3) is set to logical 1, and further requests will not be sent. Drum Controller will give up and become ready, see DRC 001, 002.

3.5. High-Speed Bus.

Transports of data words via the high-speed data bus are initiated by a Cycle Stealing Request from the controller, see fig. 6. During writing, the CYS Request is sent one word time before the specified word location reaches the read/write head. During reading, the CYS Request is transmitted two-bit's time after the word has passed the head. In both cases, the central processor has to reply on the call, first by asking for the core store address and the direction of the data transfer, and then by sending a signal, HDCGiData, indicating the time interval in which data are to be gated on the high-speed bus, see DRC 030, 031. The whole procedure has to be terminated within 18 microseconds, otherwise it is too late. To prevent damage to the core store in case of bus overloading, the procedure is supervised, and, in case that the procedure is still in operation at the time it is too late for correct data handling, then the address and the data situation are frozen, the block transfer interrupted, no more CYS Requests transmitted, and Status(3) set to logical 1 indicating data overrun.

4. ADJUSTMENTS.

Two timing systems have to be adjusted in the DRC 401 controller: The basic clock pulse system which divides the bit time into four time intervals, and the speed control system which supervises the drum speed. Before any adjustments are carried out, the drum should have been running at least one hour to obtain thermal balance in the mechanical system so that the drum speed hereafter can be considered as constant.

4.1. Adjusting the Clock Pulses.

The Clock Pulses, Time 000t150, Time 200t350, Time 400t550, and Time 600t750 are to begin with adjusted so that their leading edges divide a bit time into 4 equal time intervals, see fig. 8 and DRC 006. Ta, Tb, and Tc are adjusted by means of potentiometers A, B, and C on the RC 0909-1M in position 5, and the trailing edge of the signal on testpoint D is adjusted with the potentiometer D. The adjustment tends to give $T_a = T_b = T_c = T_d = T_{bit}/4$. When this has been done, the final adjustment is easiestly carried out while the RC 4000 is operating and the drum store frequently used in output operation.

Adjustment procedure:

Trig the oscilloscope with signal Time 000t150 (Pos. 5 Testpoint A) and observe signal WD and \neg WD (Pos. 4 Testpoint B and C) in added mode. Adjust the timing by means of potentiometers A, B, C, and D on card position 5, so that $T_m = T_n$, $T_a = T_b$, $T_c = T_{bit}/4$, and $T_g = 50$ nanoseconds. Lock all four potentiometers.

4.2. Adjusting the Speed Control Circuit.

The Speed Control Circuit (See DRC 004) detects whether the clock frequency is higher than a certain minimum frequency f_{OK} or not. If the frequency is higher than f_{OK} , a short zero signal will set the drum speed OK flip-flop to 1, and if f is lower than f_{OK} , another zero signal will reset the drum speed flip-flop to 0. Timing diagrams for their signals are given in fig. 10. For small variations, expressed in per cent, the length of the zero pulses is given by $T = 38.4 \times (f_{OK} - f) / f_{OK}$ microseconds. At normal speed, i.e. when the

drum has been running for at least one hour to stabilize the thermal conditions, the length of T_h is adjusted to $38.4 \times 0.05 = 1.92$ microseconds. If the drum speed, hereafter, decreases below $0.95 \times$ normal speed, the signal Drum Speed OK will go to 0. See fig. 11.

Adjustment procedure:

Adjust T_e (pos. 5 Testpoint E) to 58 microseconds by means of potentiometer E on card position 5. Then adjust T_h (pos. 30 testpoint H) to 1.92 microseconds by means of potentiometer F on card position 5. Lock both potentiometers.

4.3. Adjusting the Peak Detector.

The Peak Detector Circuit (see fig. 11) can be adjusted by means of the potentiometer on the circuit card in position 3 in the VRC electronic frame. Before any adjustments are carried out, one must be sure that the data on the tracks have been written correctly, i.e. the adjustment of the timing pulses has been done accurately.

The adjustment is carried out by reading random numbers from different segments, and by using an oscilloscope to observe the negative going signal on pin 16. By adjusting the potentiometer, or perhaps even by changing the values of capacitors C9 and C11, the length of the signal can be controlled. Find the minimum value, T_{min} , and the maximum value, T_{max} , for which readings are performed without parity errors, and then adjust the time to $T = T_{min} + 0.4 \times (T_{max} - T_{min})$. A powerful program tool for this operation is the testprogram, Read Check with Acoustics Alarm. Signal waveforms with time tolerances are given in fig. 7.

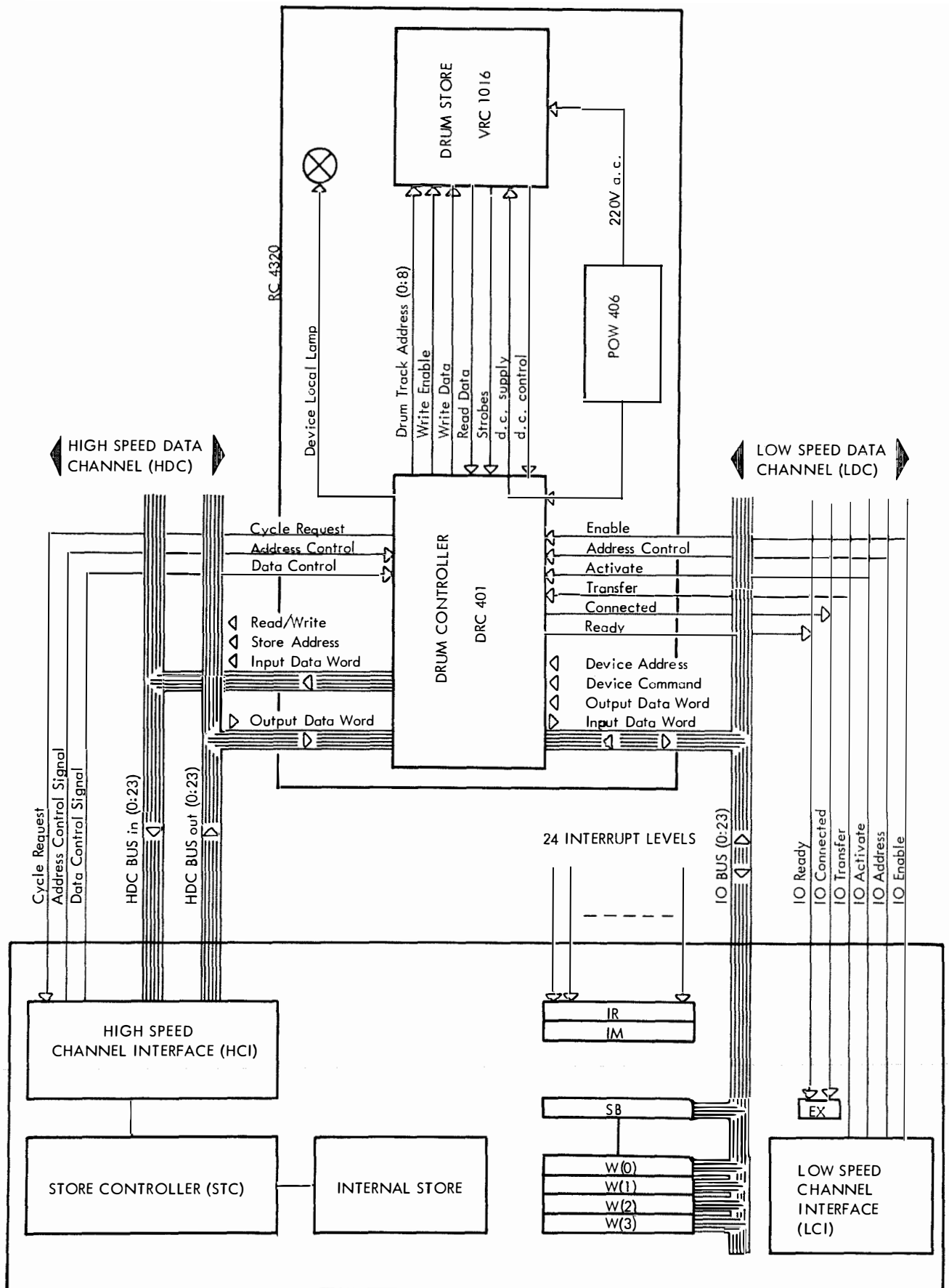


Fig. 1. Schematic diagram giving a functional description of the interconnections between the RC 4320 Computer, the Controller, and the Drum. It will be seen that RC 4320 is a standard High-Speed I/O Device controlled via the Low-Speed Channel and transferring data via the High-Speed Channel.

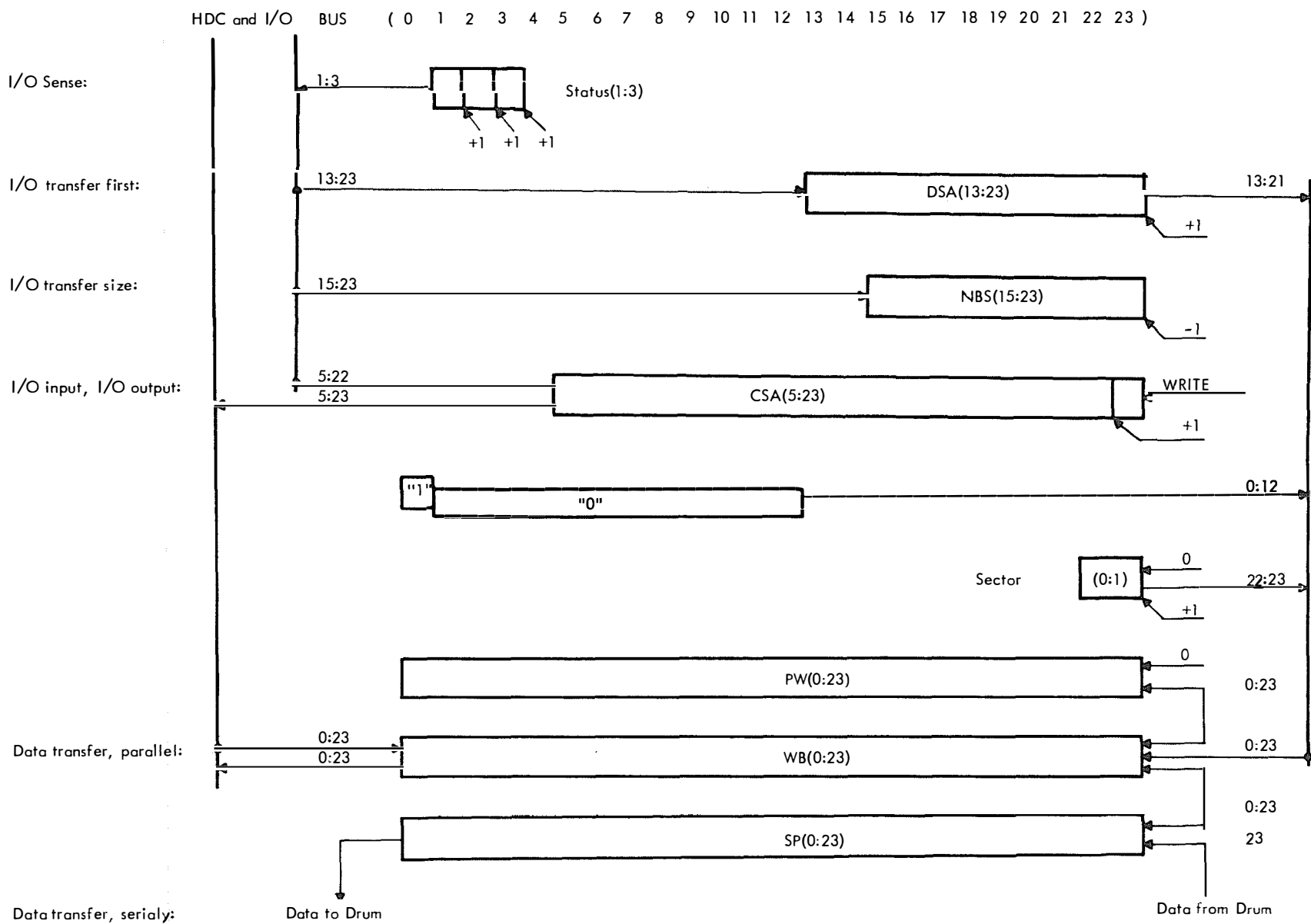


Fig. 2. Register structure for RC 4320. All registers having connections to or from Bus lines are shown as well as registers co-operating with the Word Buffer register. Other registers, such as word and bit counters or start stop logic elements, are not shown here.

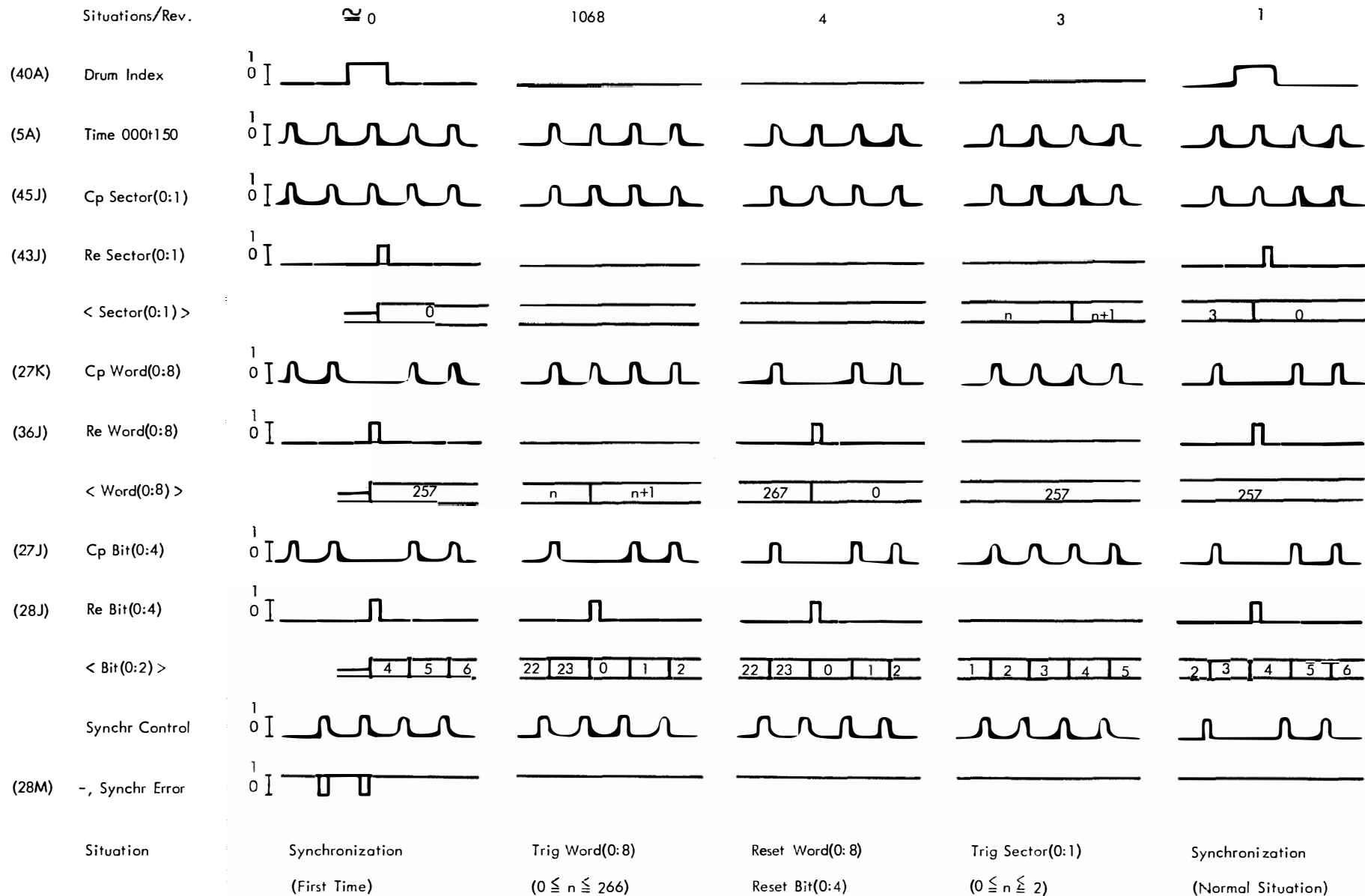
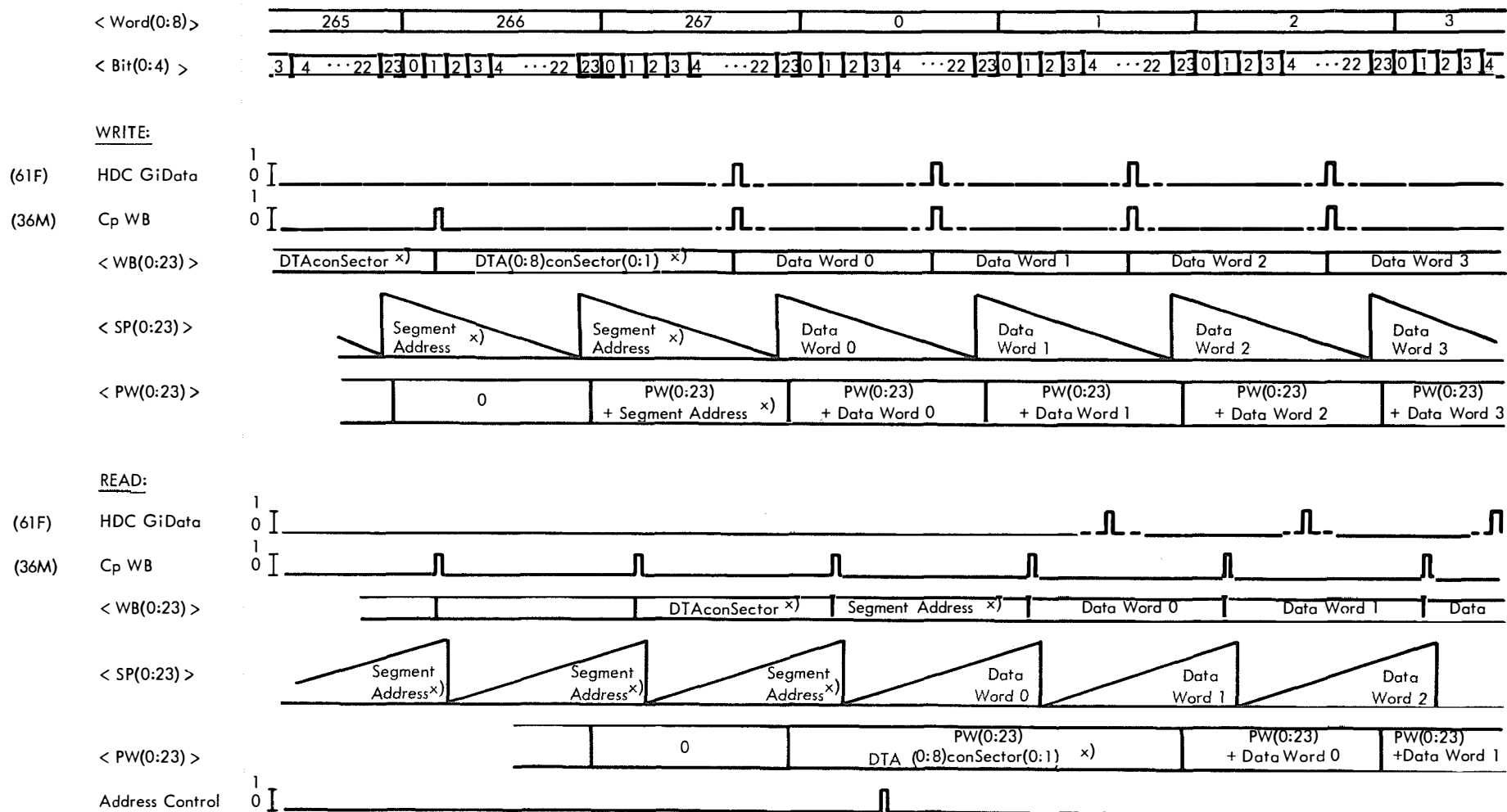


Fig. 3. Timing diagram for the Sector(0:1)conWord(0:8)conBit(0:4) register. The way it is synchronized from the drum index is indicated, and it is shown how the Sector register goes from 0 to 3, the Word register goes from 0 to 267, and the Bit register goes from 0 to 23.

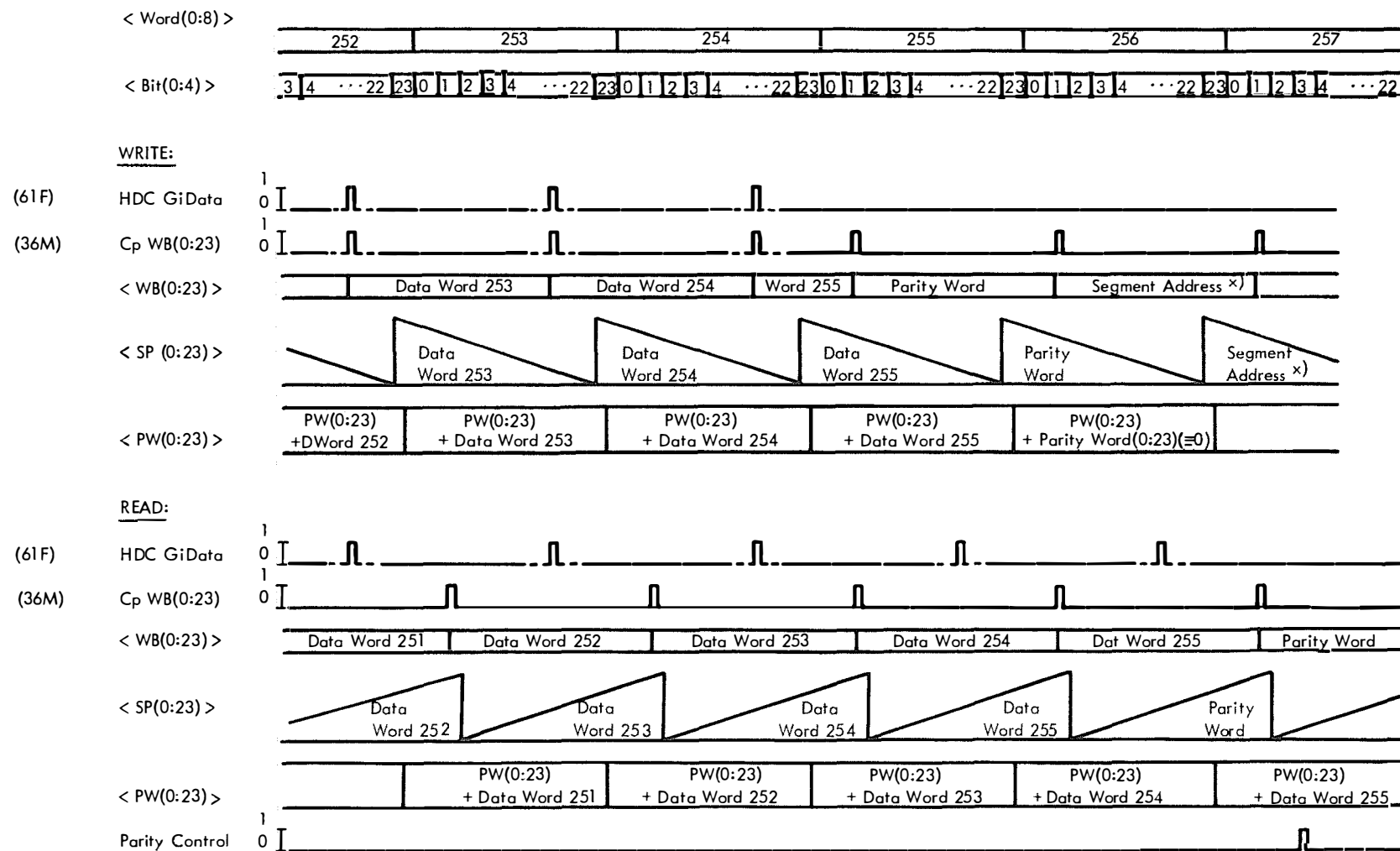
Fig. 4. Timing diagram for data transports in the beginning of segment transfer either to or from the drum. Register Word(0:8)conBit(0:4) acts as a time base. For the data registers, the contents as well as shifting times, are indicated.



x) And a "1" in position 0.

Timing Diagram for Data Transports in the beginning of a Segment.

Fig. 5. Timing diagram for data transports in the end of a segment transfer either to or from the drum. Register Word(0:8) on Bit(0:4) acts as a time base. For the data registers, the contents, as well as shifting times, are indicated.

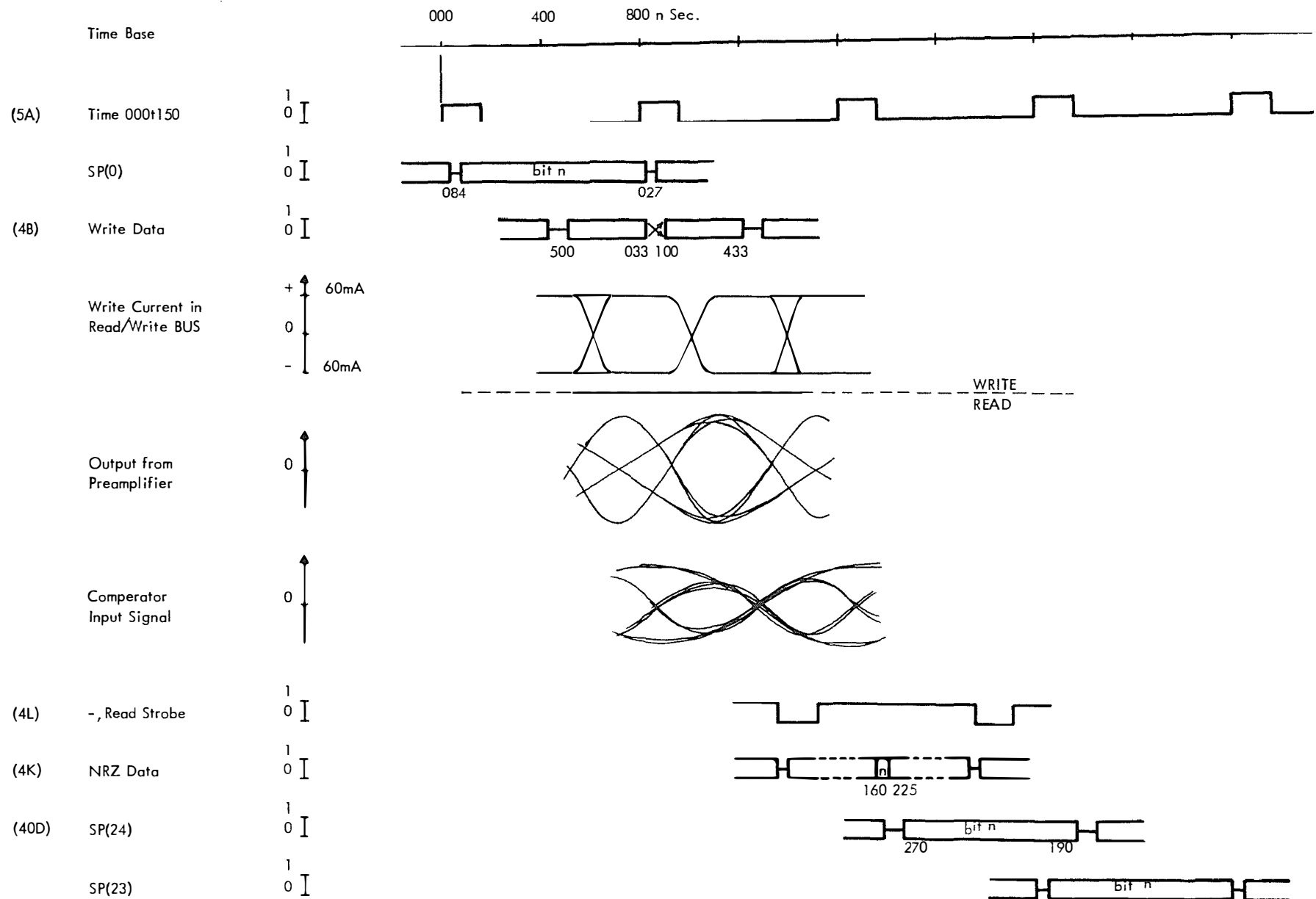


^{x)} And a "1" in position 0.

Timing Diagram for Data transports in the end of a Segment

[illegible]

Fig. 7. Timing diagram showing the wave-forms of bit n from the time it leaves the serial register SP(0) and until it enters the register SP(23) after having been stored on a track. Calculated worst case shifting times for the signals are indicated.



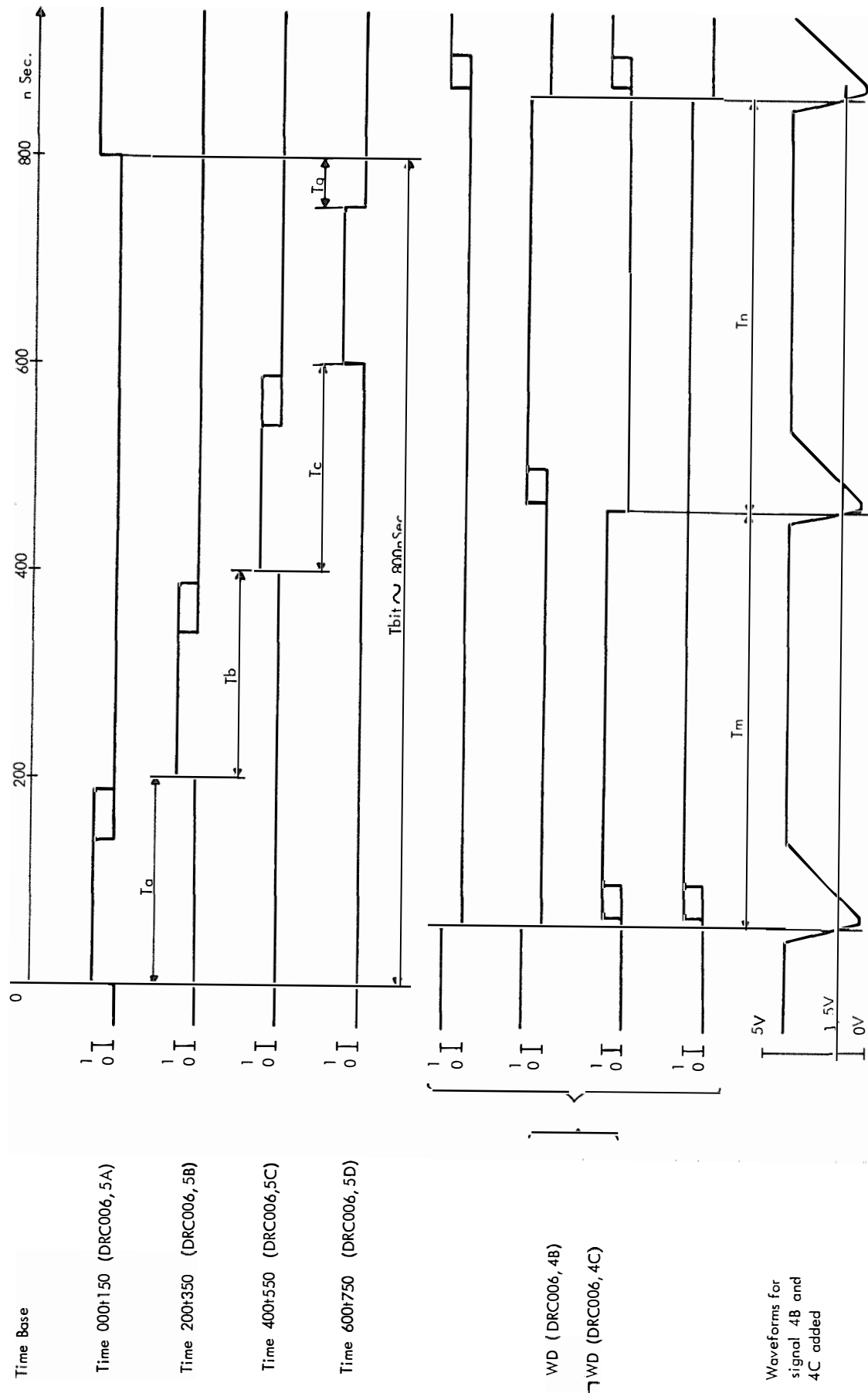


Fig. 8. Timing diagram for the clock pulse signals and the data signals to the drum. The clock pulses are always running, and their timings will correspond very nearly to the indicated values; but the exact timing depends on the waveforms of signal 4B and 4C added. Here T_m must be equal to T_n . The waveform can only be seen during writing on the drum.

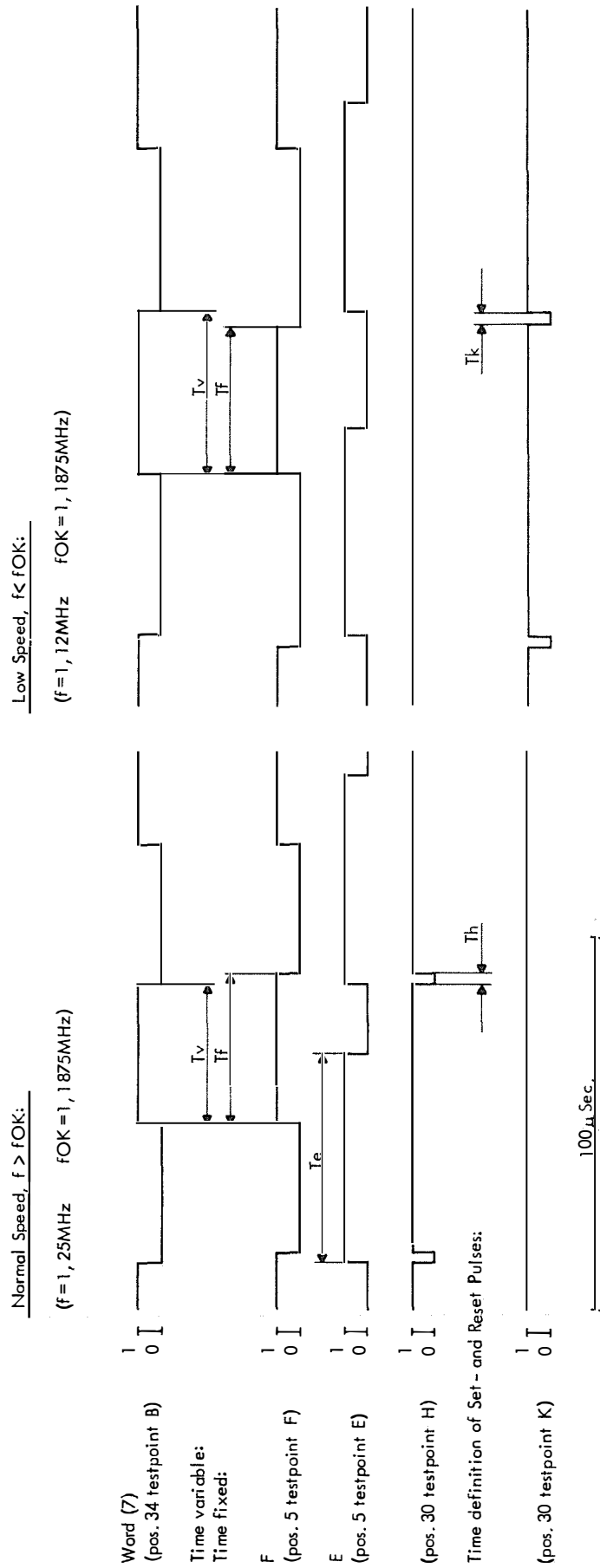


Fig. 9. Timing diagram showing the operation of the speed control circuit. Two situations are shown, one for the normal situation where the drum speed is 2880 RPM giving a clock frequency of 1,25 MHz, and one for the situation where drum speed is 10 per cent below normal.

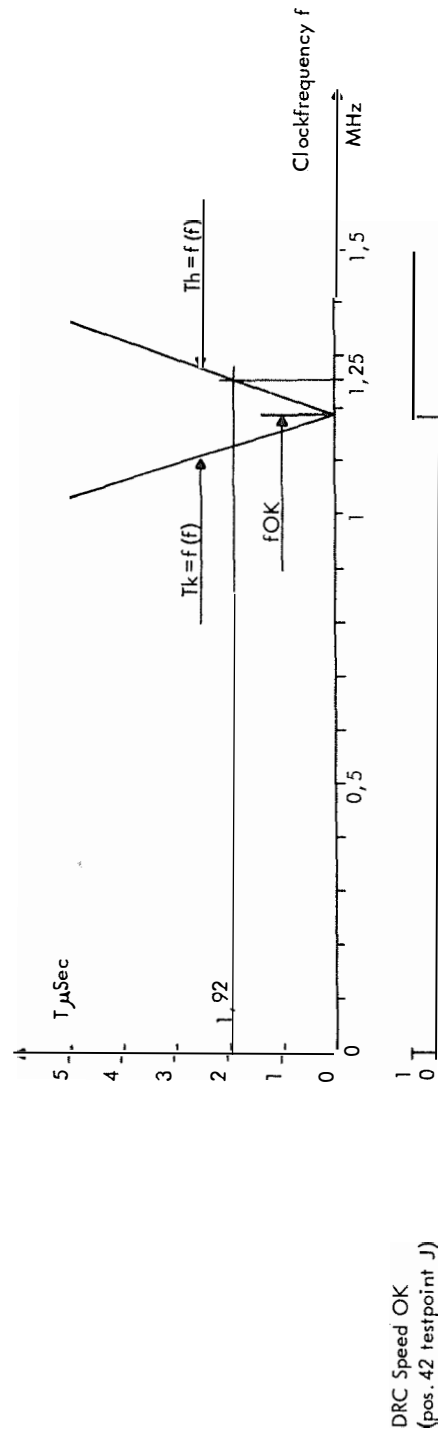
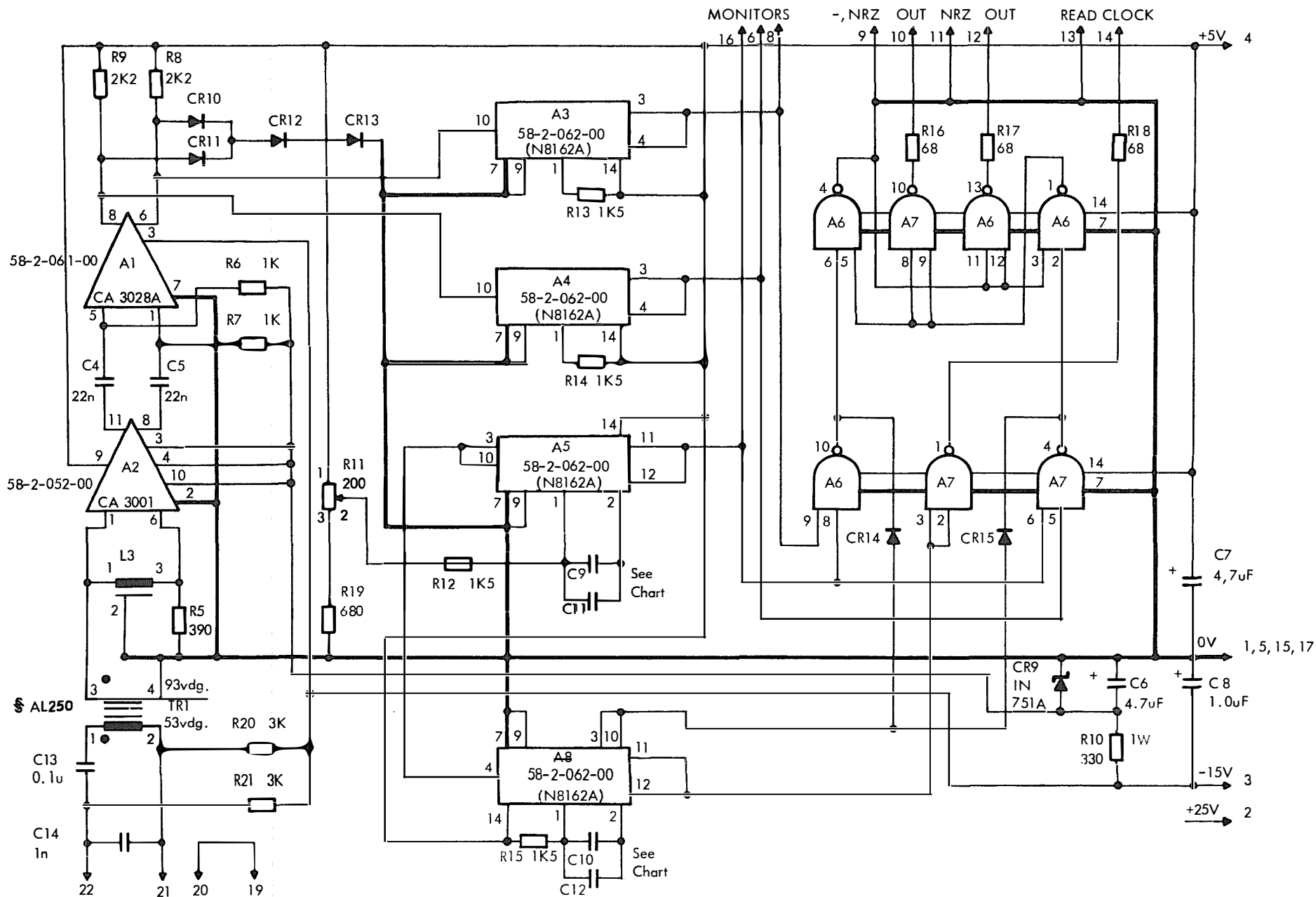


Fig. 10. The variation of the length T_n and T_k of the set and reset pulses is shown as functions of the clock frequency f . The final result from the speed control circuit is also given as a function of the frequency. It will be seen that, from not running to 95 per cent speed, the signal DRC Speed OK is logical 0, and from 95 per cent and up to 100 per cent (or more), the DRC Speed OK is logical one.

Fig. 11. Circuit diagram for the peak detector circuit card.



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MODIFICATION

OF

MODEL 1016 DRUM MEMORY

A/S REGNECENTRALEN

Falkoneralle 1

2000 COPENHAGEN F.

Temporary modification of VRC Drum type 1016 to obtain noise-free operation has been carried out by RC step-by-step as follows:

A. Taking Apart of the Electronic Card Chassis and Connector Panel

The electronic card chassis, control panel, tag board 3, and connector panel, including the multi-connectors J1, J2, J3, and J4, are taken from the rest of the drum system. These parts are sent to the assembling workshop where the following is carried out.

B. Clearing of Pin Positions

1. Remove all connection wiring from pins 13, 14, 15, and 16 on tag board 3.
2. Remove connection wiring from the electronic card chassis as follows:
 - a. On card position 1 all wiring is disconnected
 - b. On card position 2 all wiring is disconnected
 - c. On card position 3 all wiring is disconnected
 - d. On card position 4 all wiring is disconnected
 - e. On card position 5 all wiring is disconnected
 - f. On card position 6 all wiring to pins 1,2,3,4, and 29 is disconnected
 - g. On card position 7 all wiring to pins 1,2,3,4, and 29 is disconnected
 - h. On card position 8 all wiring to pins 1,2,3,4, and 29 is disconnected
 - i. On card position 9 all wiring is disconnected except the wiring on pins 26, 27, and 28
 - j. On card position 10 all wiring is disconnected except the wiring on pins 26, 27, and 28
 - k. On card position 11 all wiring is disconnected except the wiring on pins 26, 27, and 28

Now the frame is ready for wiring.

C. Wiring of Inverters

The address X selection is changed somewhat by using some of the inverters on card position 8 to generate the necessary X selection signals in both representations. (see diagram pages 5,6 for new wiring)

D. Establishment of the 0 Volt System

The 0 volt system is constructed as two 0 volt systems connected together at one point (see diagram page 7). The one 0 system is a 0 system for all circuits having digital inputs and outputs. This system incorporates card positions 1,2,3, and 9,10,11.

The other 0 system is a 0 system for all circuits handling small level analog signals plus digital circuits which are not switched during reading of a track. This system incorporates card positions 4,5,6,7, and 8.

To obtain this separation, it is necessary to rearrange some of the cards:

1. Writer fo track 0 to 255
2. Writer for track 256 to 511
3. Peak Detector
4. Read Preamplifier for 0 to 255
5. Read Preamplifier for 256 to 511
- 6.-11. Unchanged

Furthermore, it is necessary to make small changes on the Read Preamplifier Cards and Peak Detector Circuit Cards (see diagram pages 8, 9, 10, 11).

E. Establishment of +25, -15, +5 Volt System

The DC power supply system is divided into two groups in the same way as the 0 volt system. The wiring of the DC supply system is shown on pages 12, 13.

F. Establishment of Digital Inputs and Outputs

Some minor changes in the wiring of the digital signals have been made (see diagram page 14).

G. BUS Wiring

Due to the rearrangement of the cards, the BUS wiring is changed a little (see diagram page 15).

H. Circuit Card Modifications

Four circuit cards (six, if drum has more than four head bar modules) have been modified as follows:

1. Read Preamplifier for data tracks has been modified by cutting two printed wires, drilling eight more holes, and inserting eight new components. The value of resistors R19 and R20 must be equal and is approximately 3000 ohms. The exact value depends on the amplitude of the AC output which must be adjusted to 2 volt peak to peak by inserting the expedient resistors. (see diagram page 11).
2. Read Preamplifier for clock track is modified in a similar way as H.1. (see diagram page 9).
3. Peak Detector card for data track is modified by cutting some of the printed wires, changing some of the components, and adding a few other components (see diagram page 12). Some of these components have been difficult to place in a proper way, so they are fixed to the circuit card. They are more or less self-supporting.
4. Peak Detector card for clock track is modified as in H.3. (see diagram page 10).

I. Reassembling

The modification in the assembling workshop is now

I. Reassembling (cont.)

completed. The modified electronic chassis can now be reassembled with the drum plate.

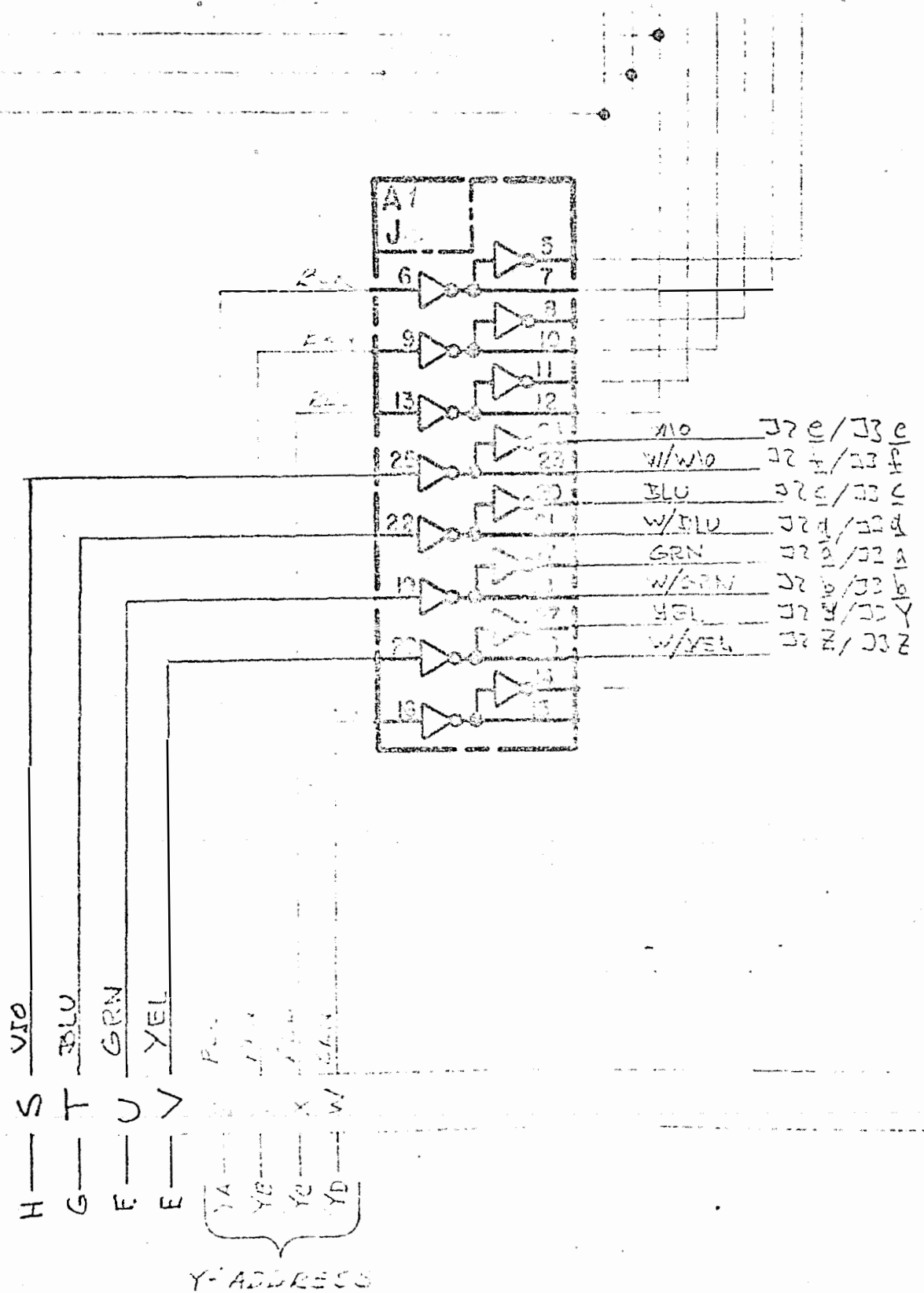
J. Removal of 0 Volt to Chassis Connection

Inside the square can, the connection between chassis and 0 volt is removed by cutting away the black wire from chassis to 0 volt on the clock preamplifier circuit card.

Now there should be no connection between the electronic system and the drum chassis.

K. Interface Cable Connection

Some changes in the wiring of the interface connection have been made (see diagram page 16).

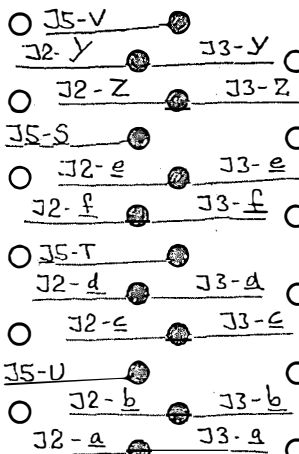


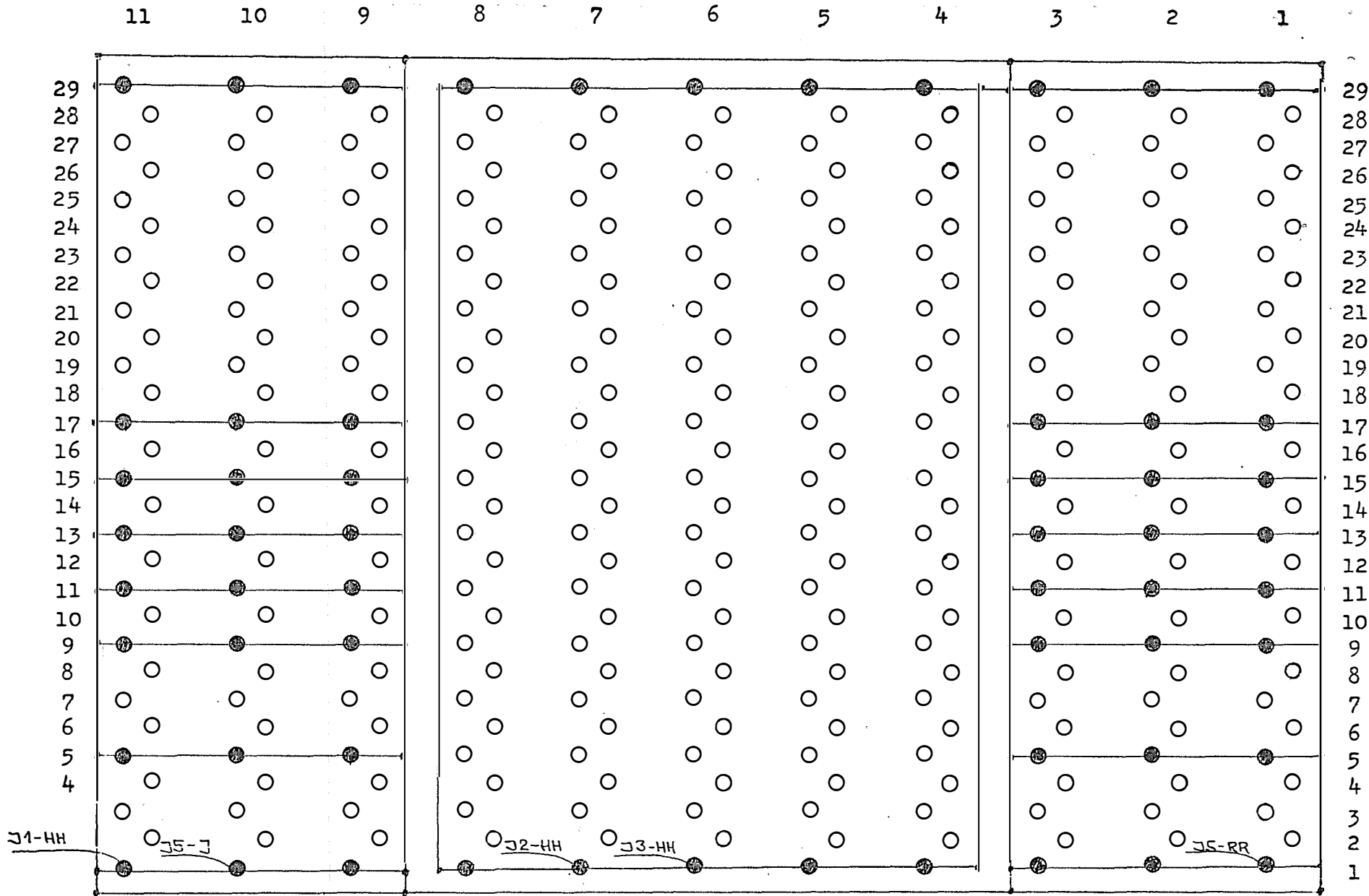
WIRING DEAGRAM FOR INVERTERS IN THE X SELECTION

VB642

WIRING SCHEME FOR THE X SELECTION INVERTERS

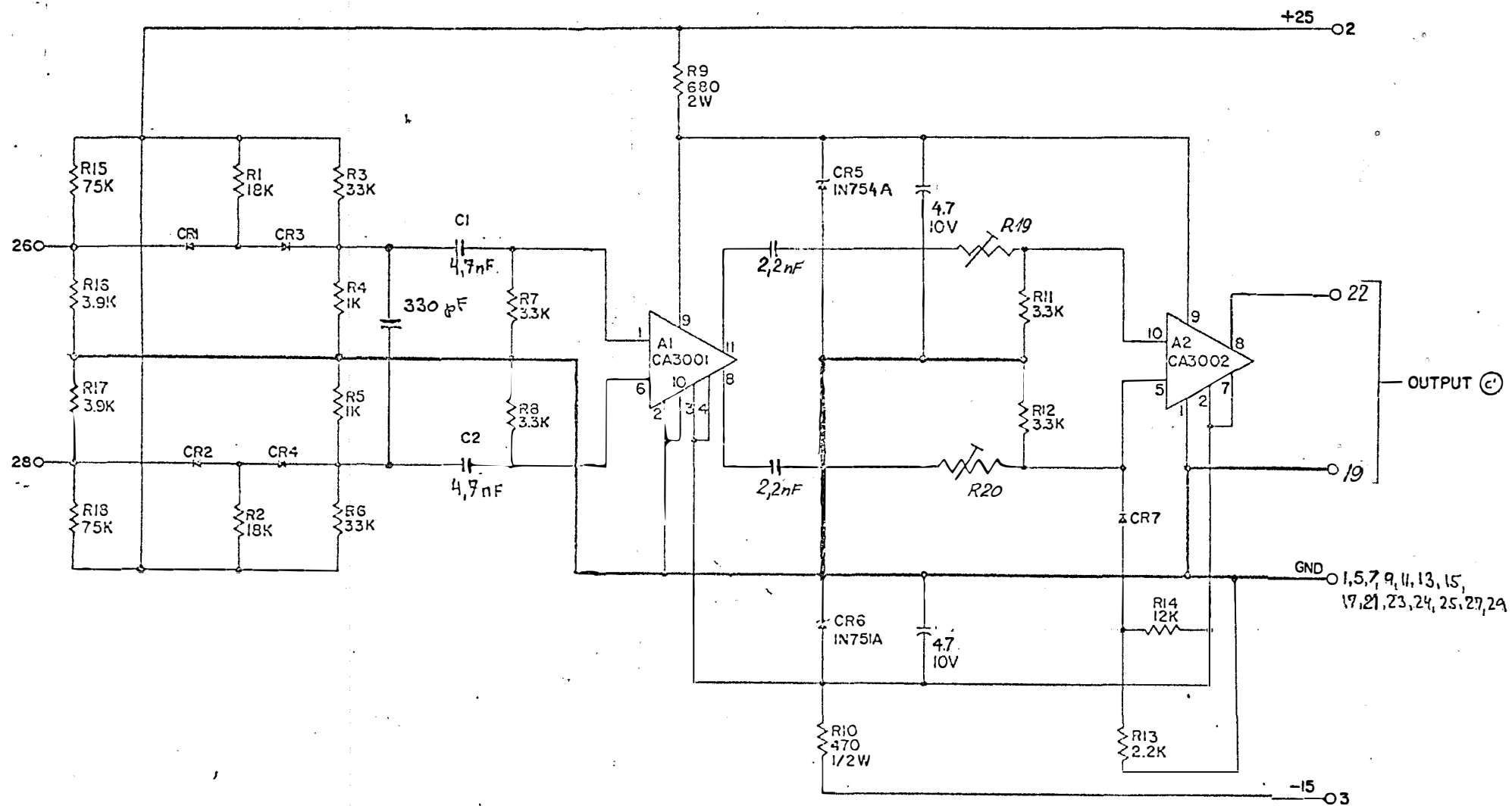
	11	10	9	8	7	6	5	4	3	2	1	
29	○	○	○	○	○	○	○	○	○	○	○	29
28	○	○	○	○	○	○	○	○	○	○	○	28
27	○	○	○	○	○	○	○	○	○	○	○	27
26	○	○	○	○	○	○	○	○	○	○	○	26
25	○	○	○	○	○	○	○	○	○	○	○	25
24	○	○	○	○	○	○	○	○	○	○	○	24
23	○	○	○	○	○	○	○	○	○	○	○	23
22	○	○	○	○	○	○	○	○	○	○	○	22
21	○	○	○	○	○	○	○	○	○	○	○	21
20	○	○	○	○	○	○	○	○	○	○	○	20
19	○	○	○	○	○	○	○	○	○	○	○	19
18	○	○	○	○	○	○	○	○	○	○	○	18
17	○	○	○	○	○	○	○	○	○	○	○	17
16	○	○	○	○	○	○	○	○	○	○	○	16
15	○	○	○	○	○	○	○	○	○	○	○	15
14	○	○	○	○	○	○	○	○	○	○	○	14
13	○	○	○	○	○	○	○	○	○	○	○	13
12	○	○	○	○	○	○	○	○	○	○	○	12
11	○	○	○	○	○	○	○	○	○	○	○	11
10	○	○	○	○	○	○	○	○	○	○	○	10
9	○	○	○	○	○	○	○	○	○	○	○	9
8	○	○	○	○	○	○	○	○	○	○	○	8
7	○	○	○	○	○	○	○	○	○	○	○	7
6	○	○	○	○	○	○	○	○	○	○	○	6
5	○	○	○	○	○	○	○	○	○	○	○	5
4	○	○	○	○	○	○	○	○	○	○	○	4
3	○	○	○	○	○	○	○	○	○	○	○	3
2	○	○	○	○	○	○	○	○	○	○	○	2
1	○	○	○	○	○	○	○	○	○	○	○	1





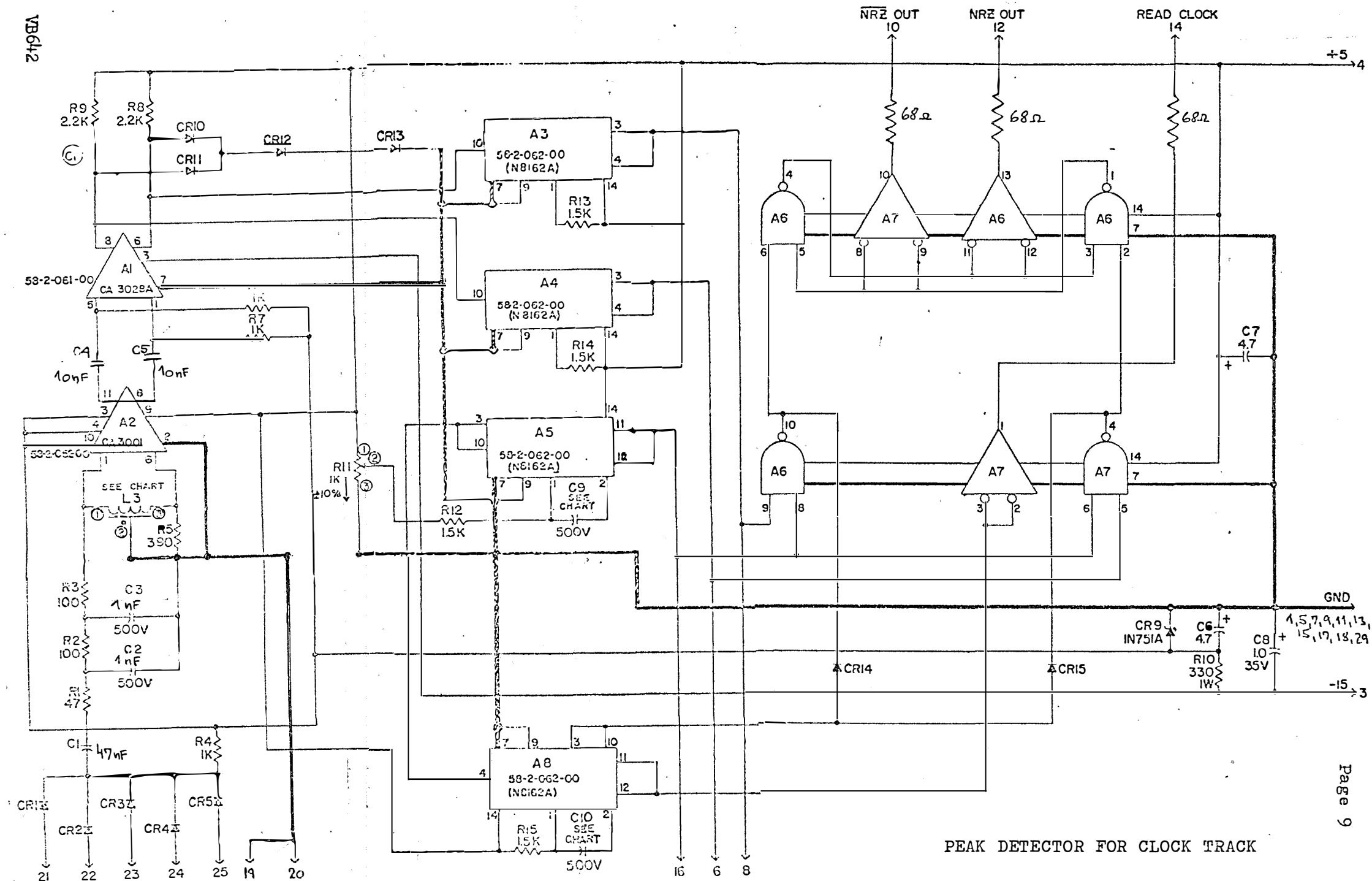
WIRING OF 0 VOLT

VB642

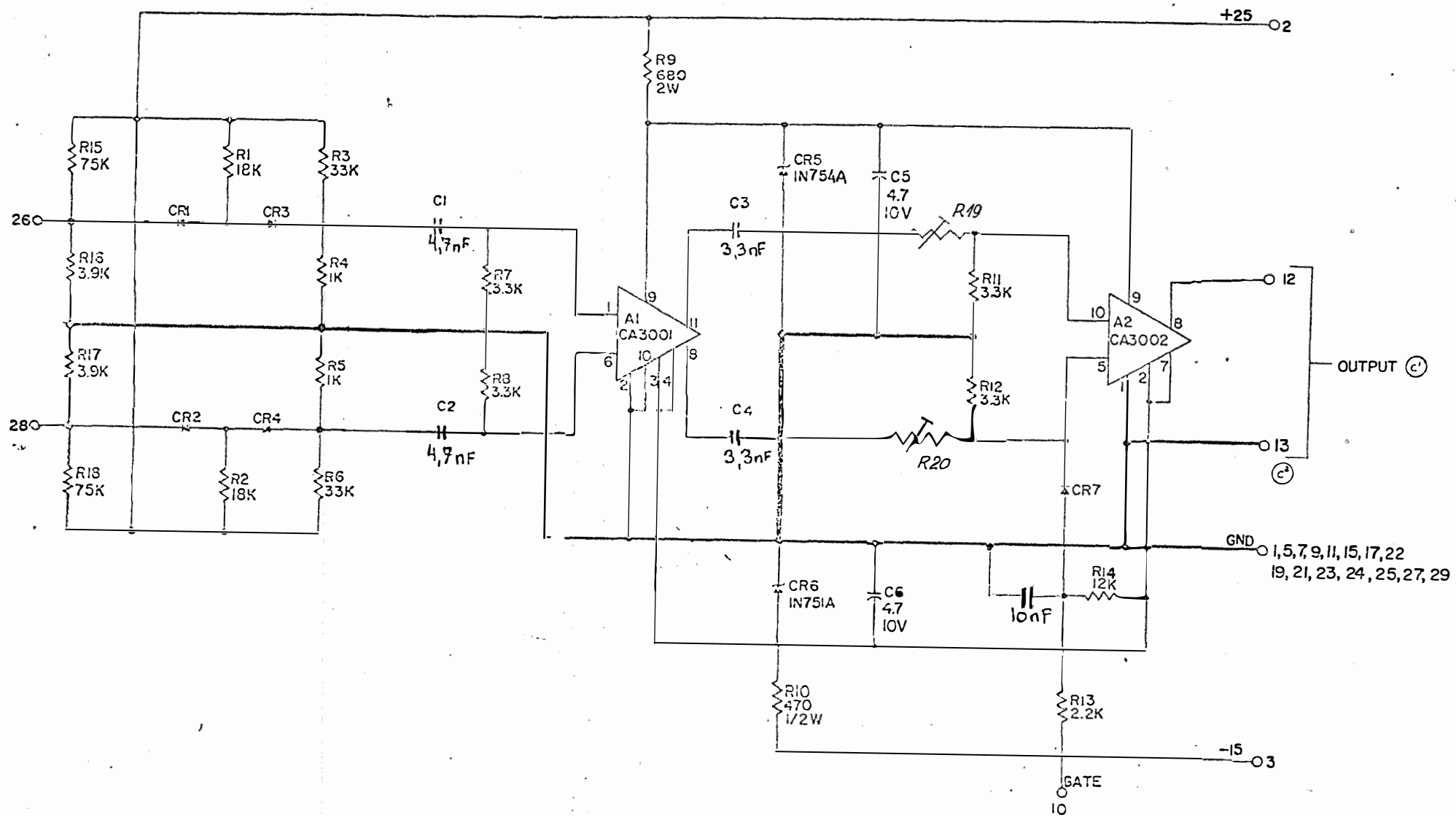


VB642

READ PREAMPLIFIER FOR CLOCK TRACK

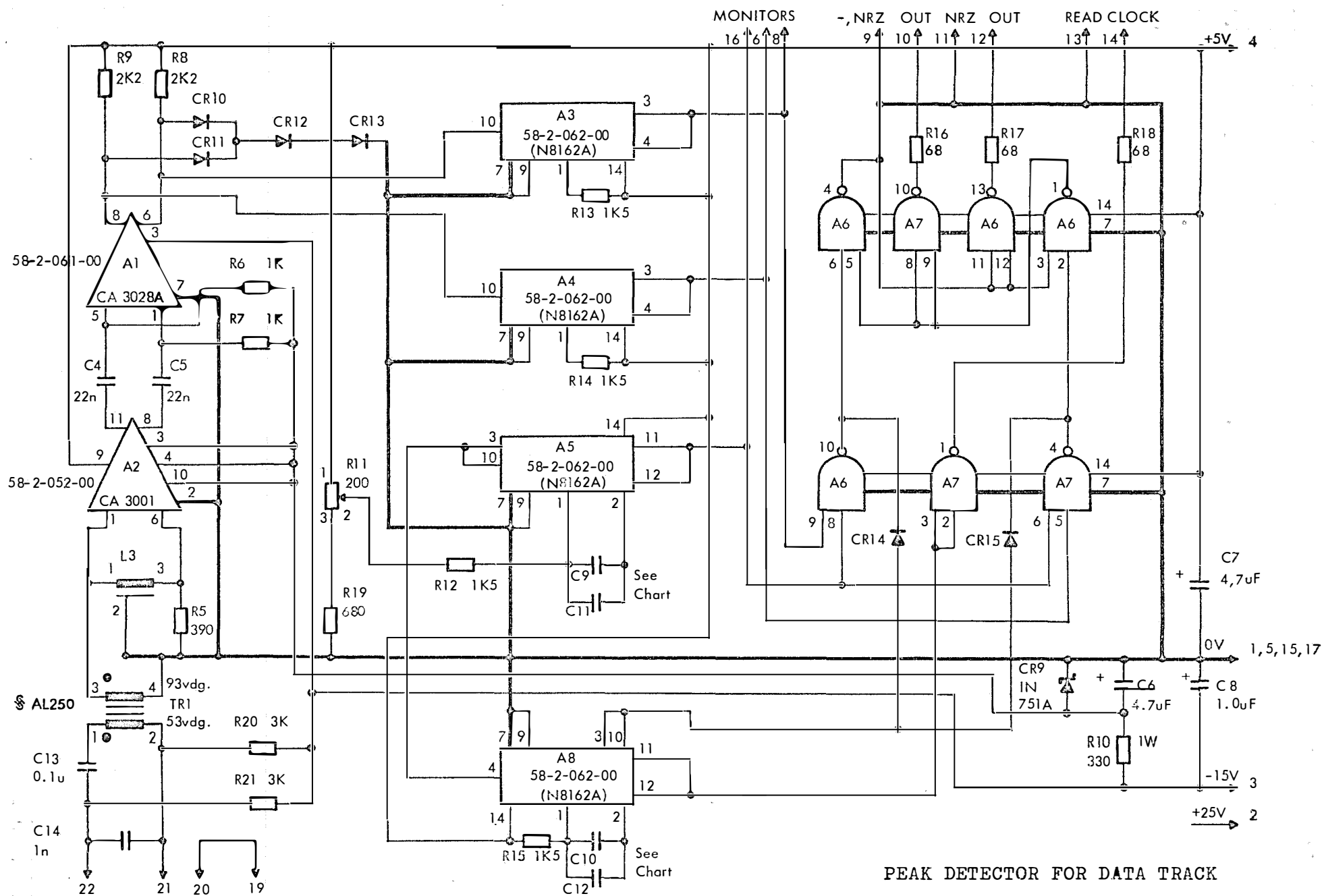


PEAK DETECTOR FOR CLOCK TRACK



V11620

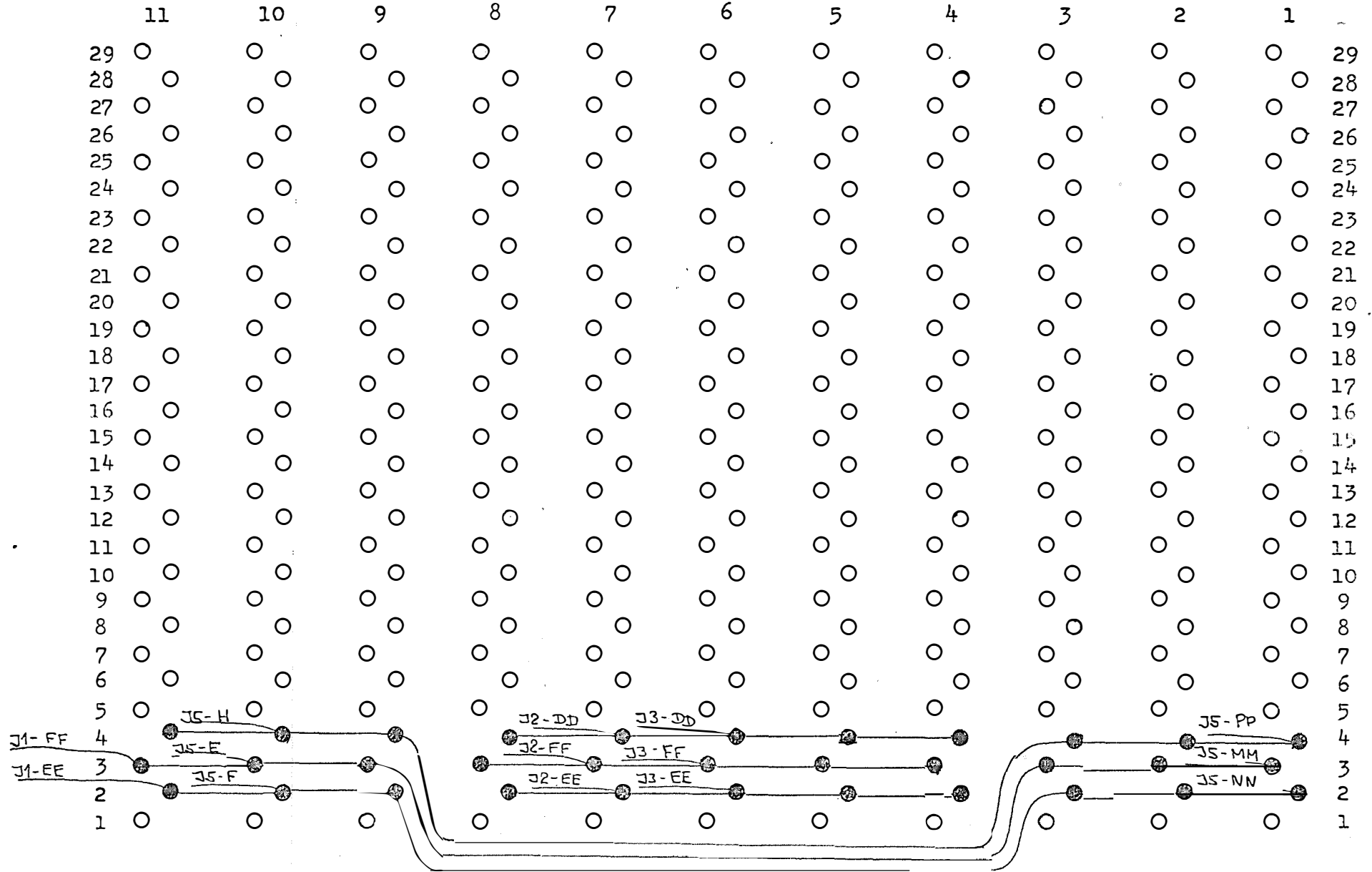
VRC1016

PEAK DETECTOR
Logic Diagram

PEAK DETECTOR FOR DATA TRACK

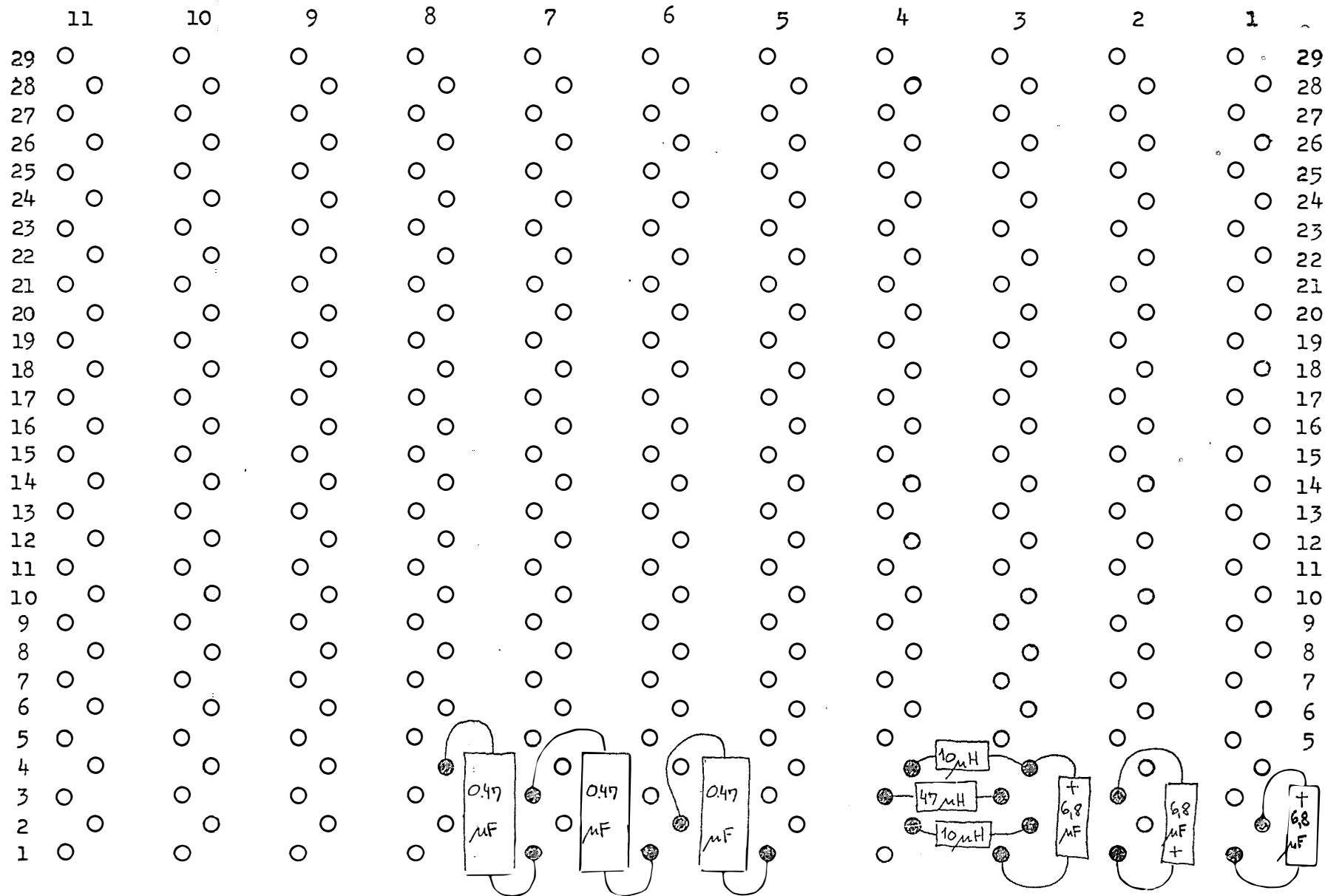
VB642

WIRING OF DC SUPPLY



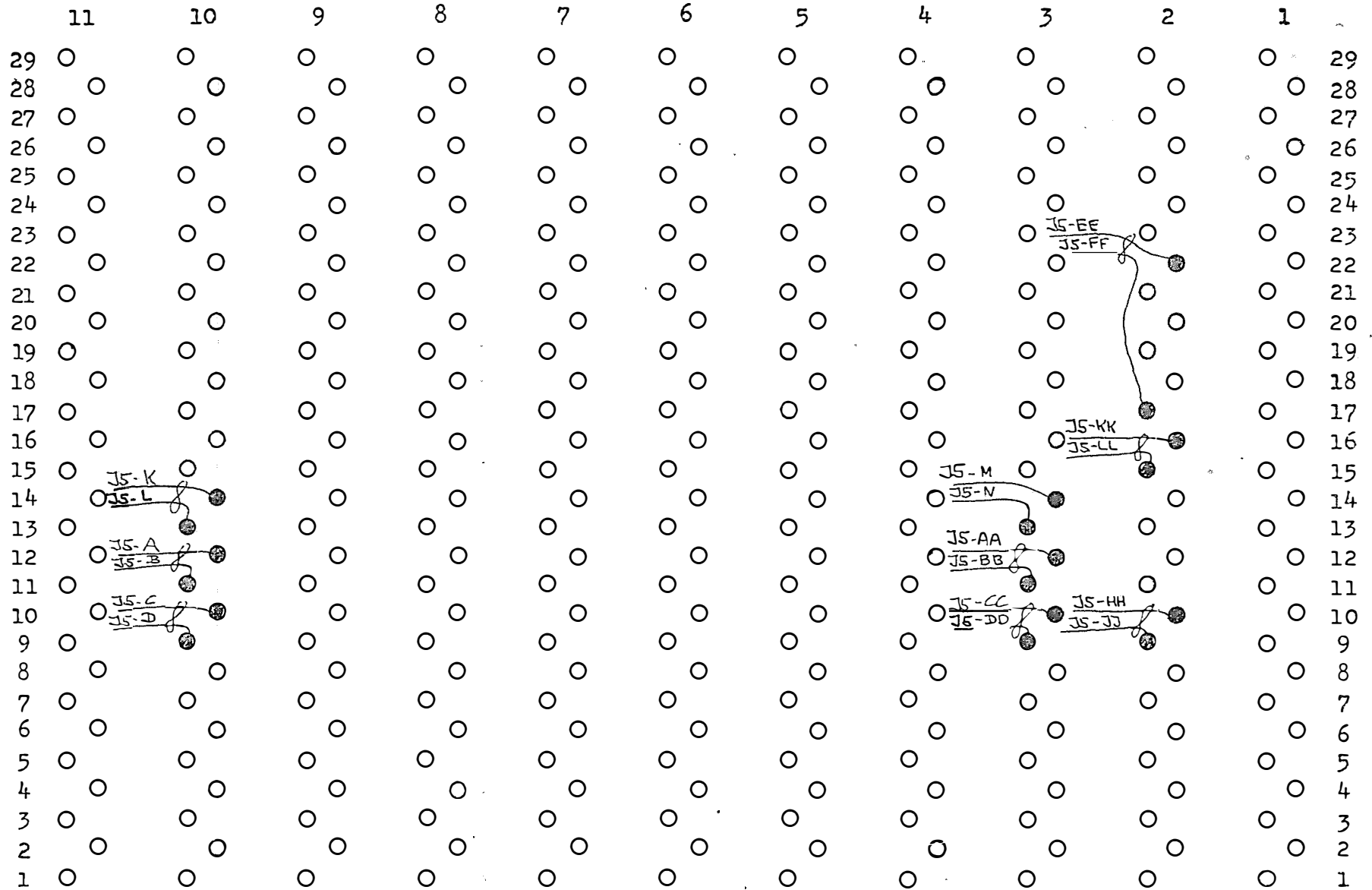
VB642

DECOUPLING COMPONENTS IN THE WIRING



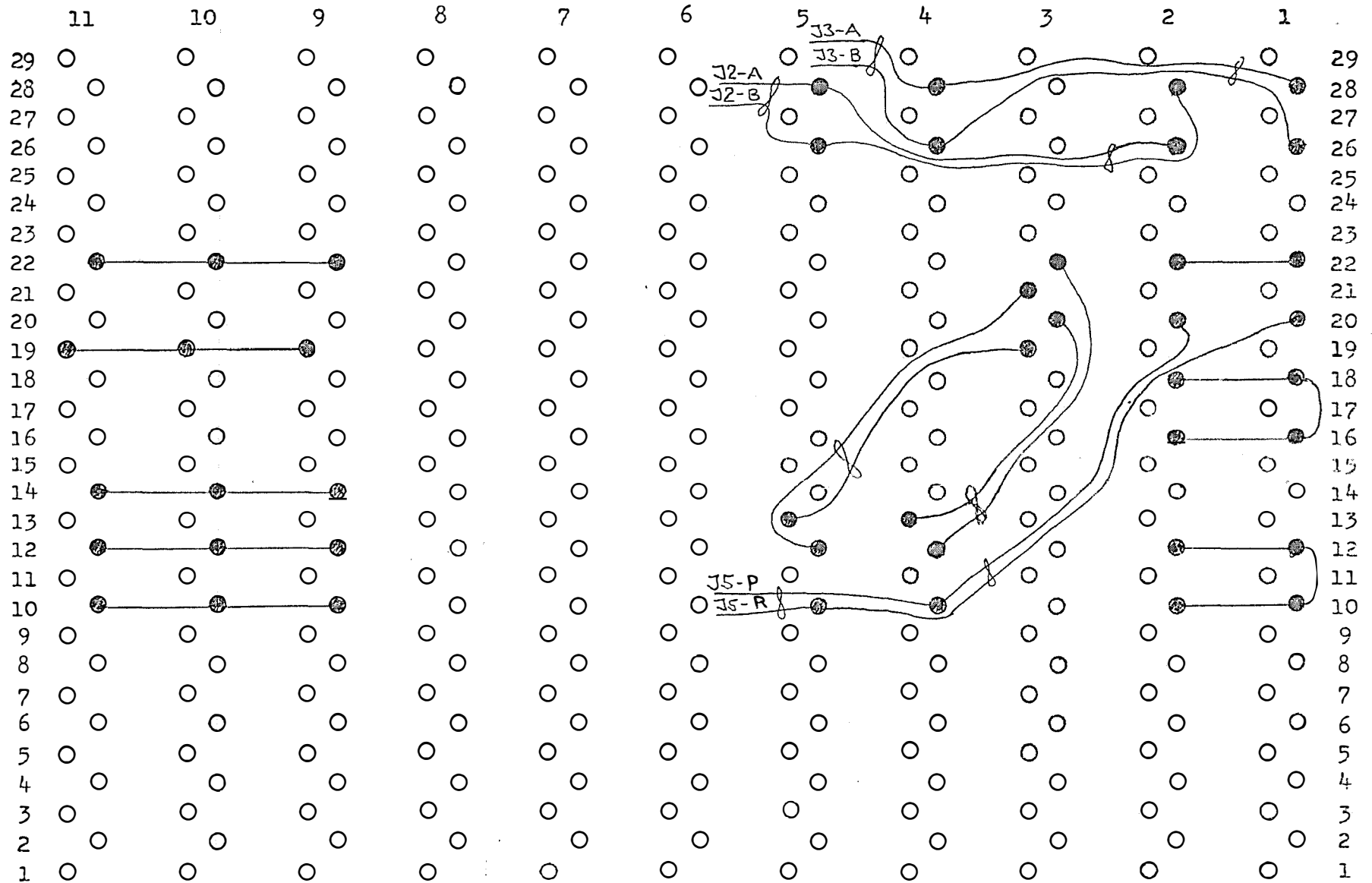
VB642

WIRING OF INPUT - OUTPUT SIGNALS



VB642

BUS WIRINGS



<u>CONNECTOR:</u> 1307			<u>CONNECTOR:</u> J5	
<u>UNIT</u> : DRC401				
<u>NAME</u>	<u>COMMENTS</u>	<u>PIN</u>	<u>NAME</u>	<u>COMMENTS</u>
NRZ DATA	FROM CLOCK TRACK	A	NRZ DATA	FROM CLOCK TRACK
-Grd.-	-	B	-Grd.-	-
-,NRZ DATA	FROM CLOCK TRACK	C	-,NRZ DATA	FROM CLOCK TRACK
-Grd.-	-	D	-Grd.-	-
MINUS 15 VOLT	RETURN	E	-15	RETURN
PLUS 25 VOLT	RETURN	F	+25	RETURN
PLUS 5 VOLT	RETURN	H	+5	RETURN
NUL VOLT	RETURN	J	0	RETURN
READ STROBE	FROM CLOCK TRACK	K	READ STROBE	FROM CLOCK TRACK
-Grd.-	-	L	-Grd.-	-
READ STROBE	FROM DATA TRACK	M	READ STROBE	FROM DATA TRACK
-Grd.-	-	N	-Grd.-	-
DTA(0)	256	P	J	BAR:EFGH
-,DTA(0)	-,256	R	-,J	BAR:ABCD
DTA(1)	128	S	H	X8
DTA(2)	64	T	G	X4
DTA(3)	32	U	F	X2
DTA(4)	16	V	E	X1
DTA(5)	8	W	YD	Y8
DTA(6)	4	X	YC	Y4
DTA(7)	2	Y	YB	Y2
DTA(8)	1	Z	YA	Y1
NRZ DATA	FROM DATA TRACK	AA	NRZ DATA	FROM DATA TRACK
-Grd.-	-	BB	-Grd.-	-
-,NRZ DATA	FROM DATA TRACK	CC	-,NRZ DATA	FROM DATA TRACK
-Grd.-	-	DD	-Grd.-	-
WE	WRITE ENABLE	EE	WRITE ENABLE	WE
-Grd.-	-	FF	-Grd.-	-
WD	WRITE DATA	HH	WRITE DATA	WD
-Grd.-	-	JJ	-Grd.-	-
-,WD	-,WRITE DATA	KK	-,WRITE DATA	-,WD
-Grd.-	-	LL	-Grd.-	-
-15V	POWER F.POW406	MM	-15V	POWER
+25V	POWER F.POW406	NN	+25V	POWER
+5V	POWER F.POW406	PP	+5V	POWER
OV	POWER F.POW406	RR	OV	POWER
Chassis	SCREN	SS	CHASSIS	FRAME
Chassis	SCREN	TT	CHASSIS	FRAME

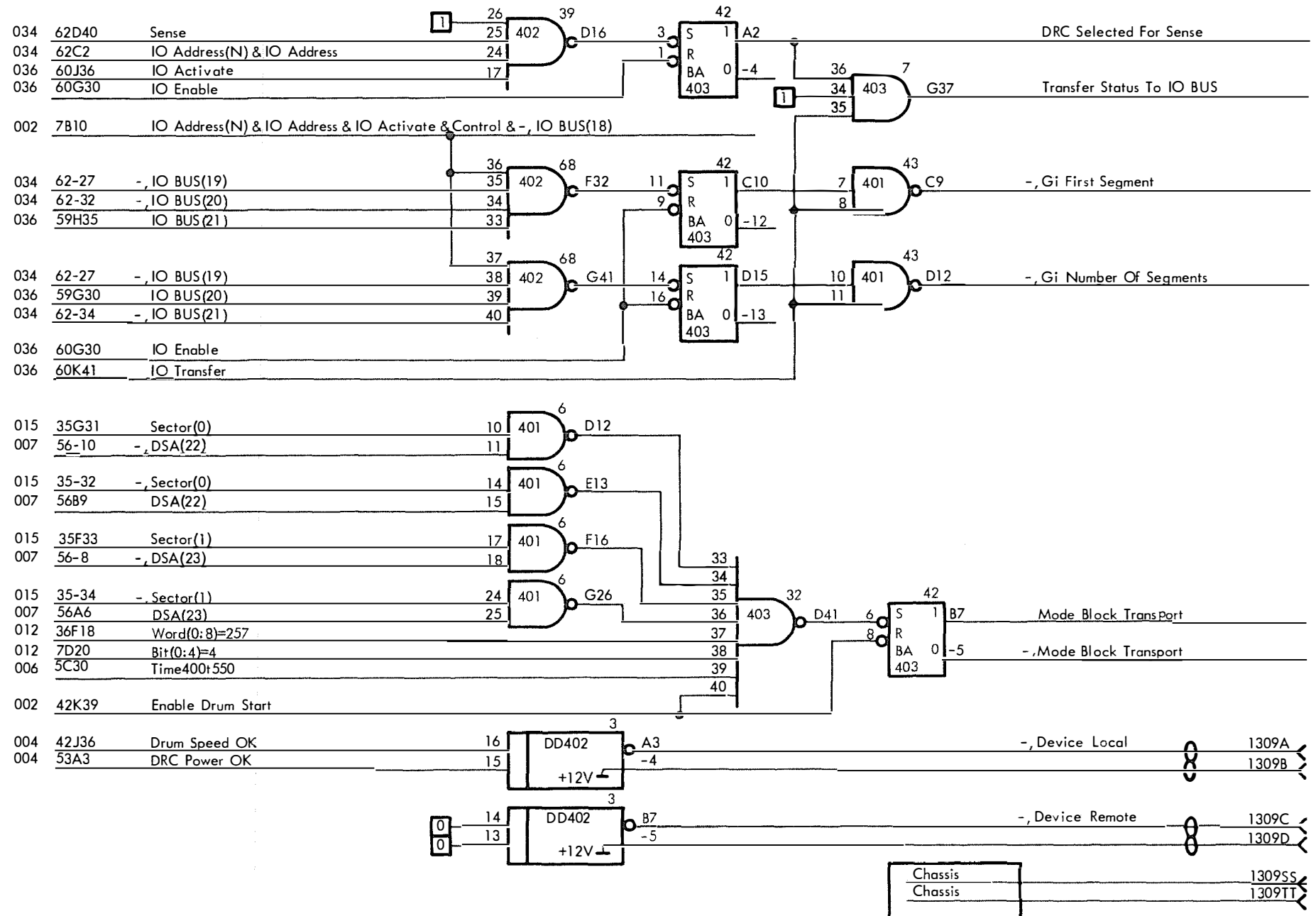
RC 4005 LOGIC DIAGRAMSDRC401Drum Controller (DRC)Dwg. No.

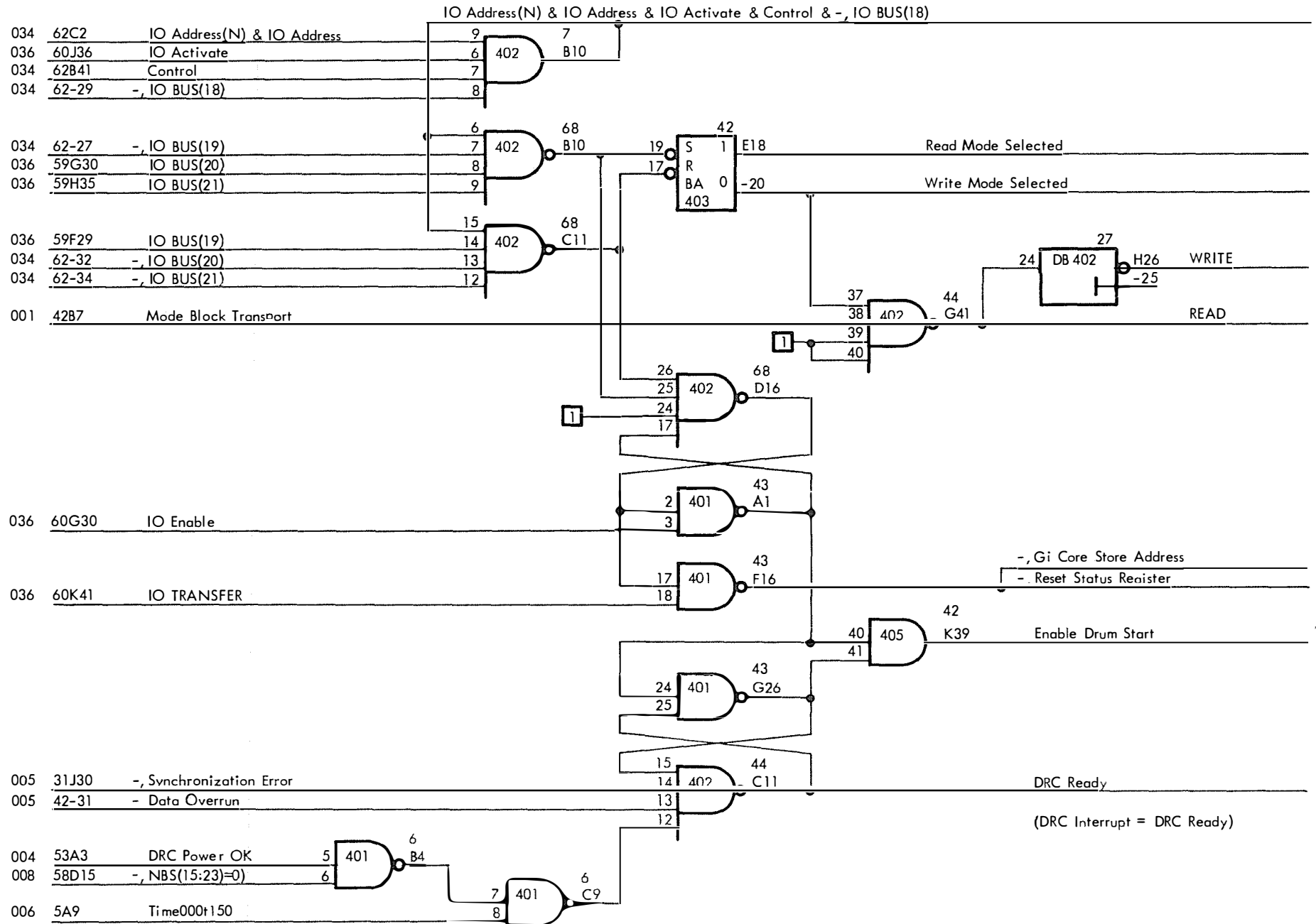
DRC001	IO COMMANDS AND MODE BLOCK TRANSPORT	V11456
002	READ/WRITE AND READY	V11457
003	CYCLE CALL	V11458
004	CONNECTED AND POWER OK	V11459
005	STATUS REGISTER	V11460
006	DRUM DATA SIGNALS	V11573
007	DRUM SEGMENT ADDRESS, DSA(12:23)	V11462
008	NUMBER OF SEGMENTS, NBS(15:23)	V11463
009	CORE STORE ADDRESS, CSA(5:10)	V11464
010	CORE STORE ADDRESS, CSA(11:23)	V11465
012	BIT AND WORD REGISTER DECODINGS	V11466
013	CONTROL SIGNALS FOR BIT, WORD, SECTOR, DSA, NBS, AND CSA	V11467
014	WORD(0:8)	V11468
015	BIT(0:4) AND SECTOR(0:1)	V11469
016	CONTROL SIGNALS FOR WORD BUFFER	V11470
017	CONTROL SIGNALS FOR PARITY WORD, AND SERIAL PARALLEL REGISTER	V11471
018	WORD BUFFER, WB(0:7)	V11472
019	WORD BUFFER, WB(8:15)	V11473
020	WORD BUFFER, WB(16:23)	V11474
021	DRUM TRACK ADDRESS, DTA(0:8), AND ENABLING OF CONTROLS	V11569
023	DRUM ADDRESS SIGNALS, DTA(0:8)	V11571
024	LOGICAL DIAGRAM	V11770
030	HDS BUSin(0:15)	V11477
031	HDC BUSin(16:23), AND HDC CONTROL	V11478

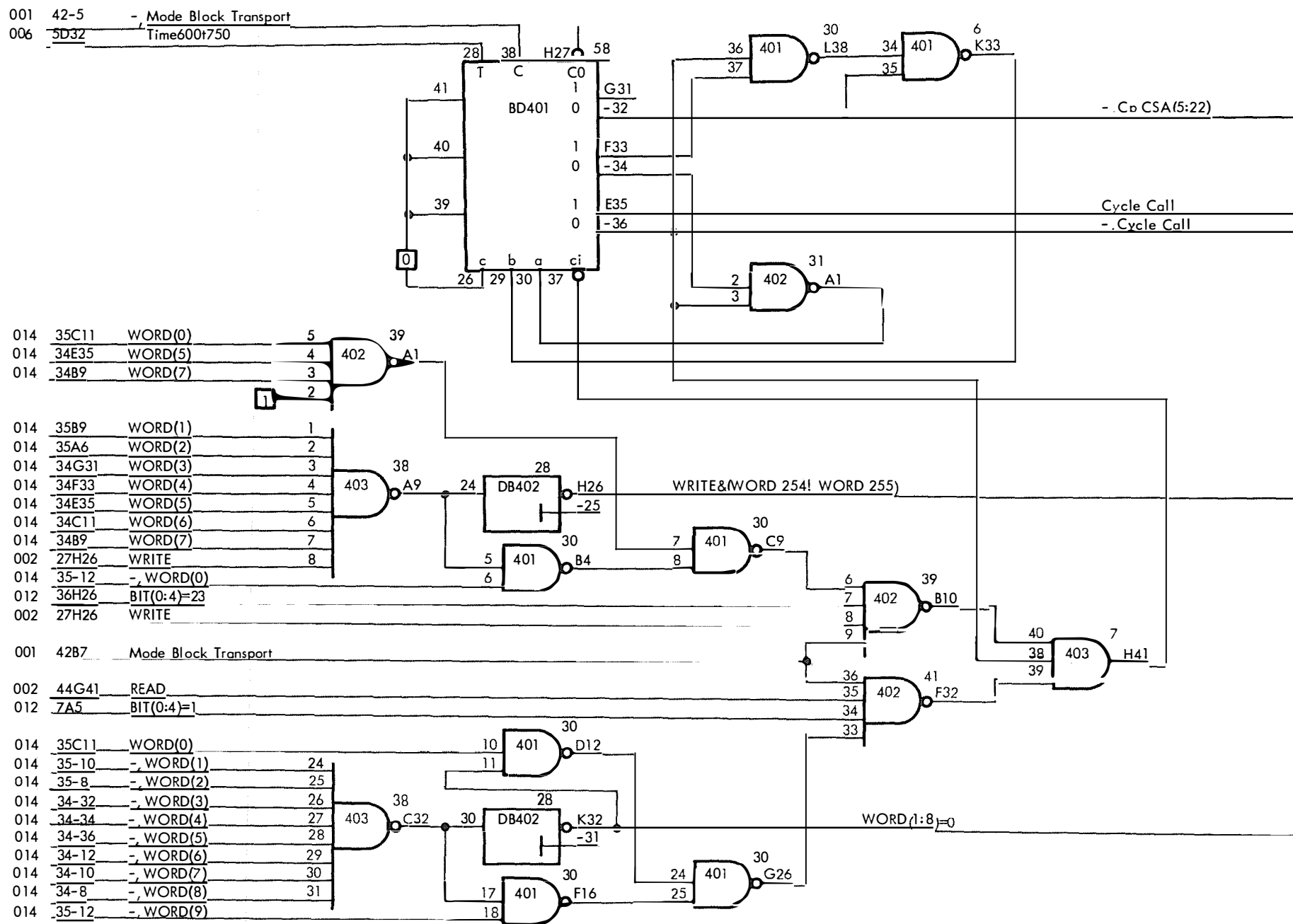
Drum Controller (DRC)

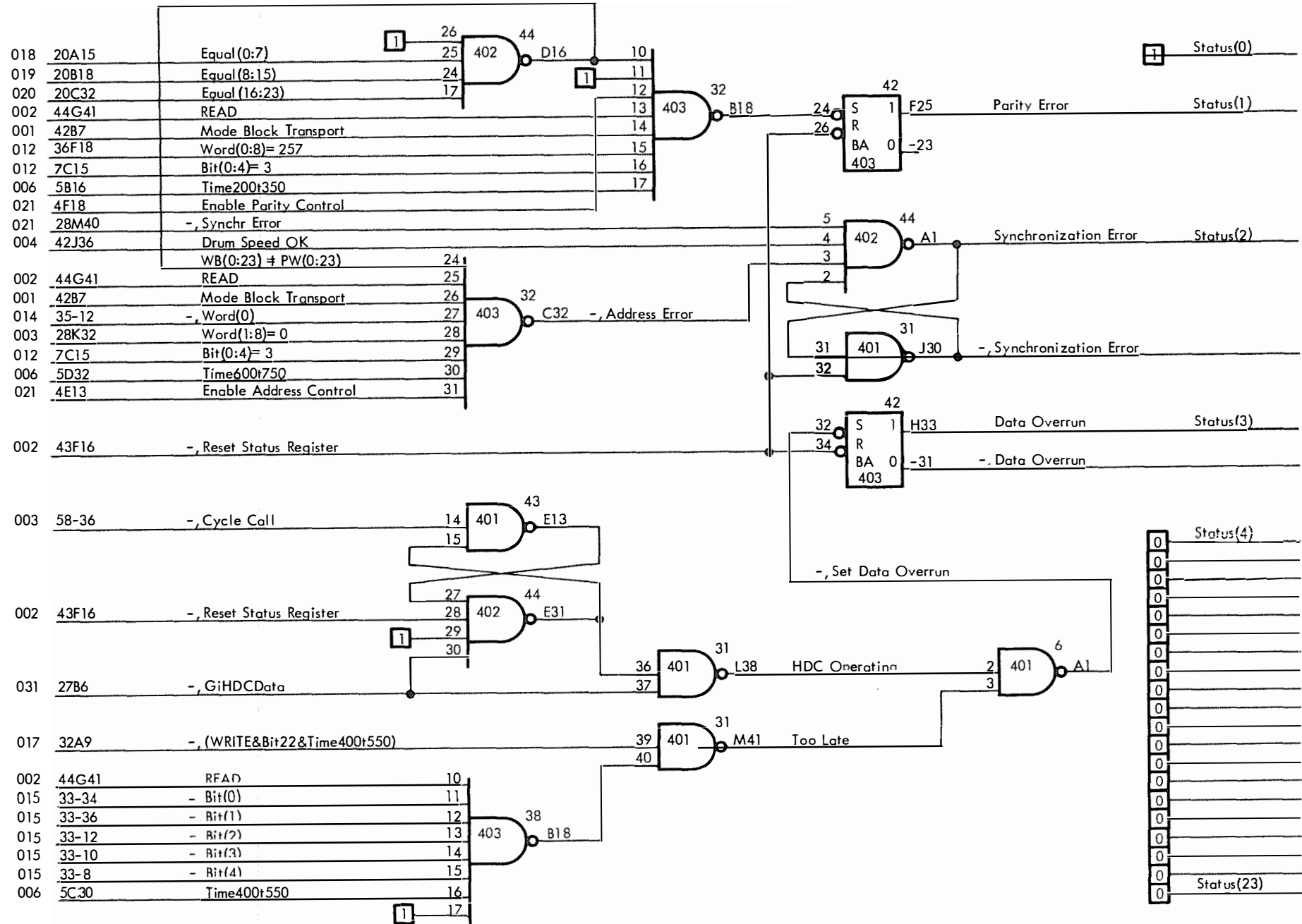
Dwg. No.

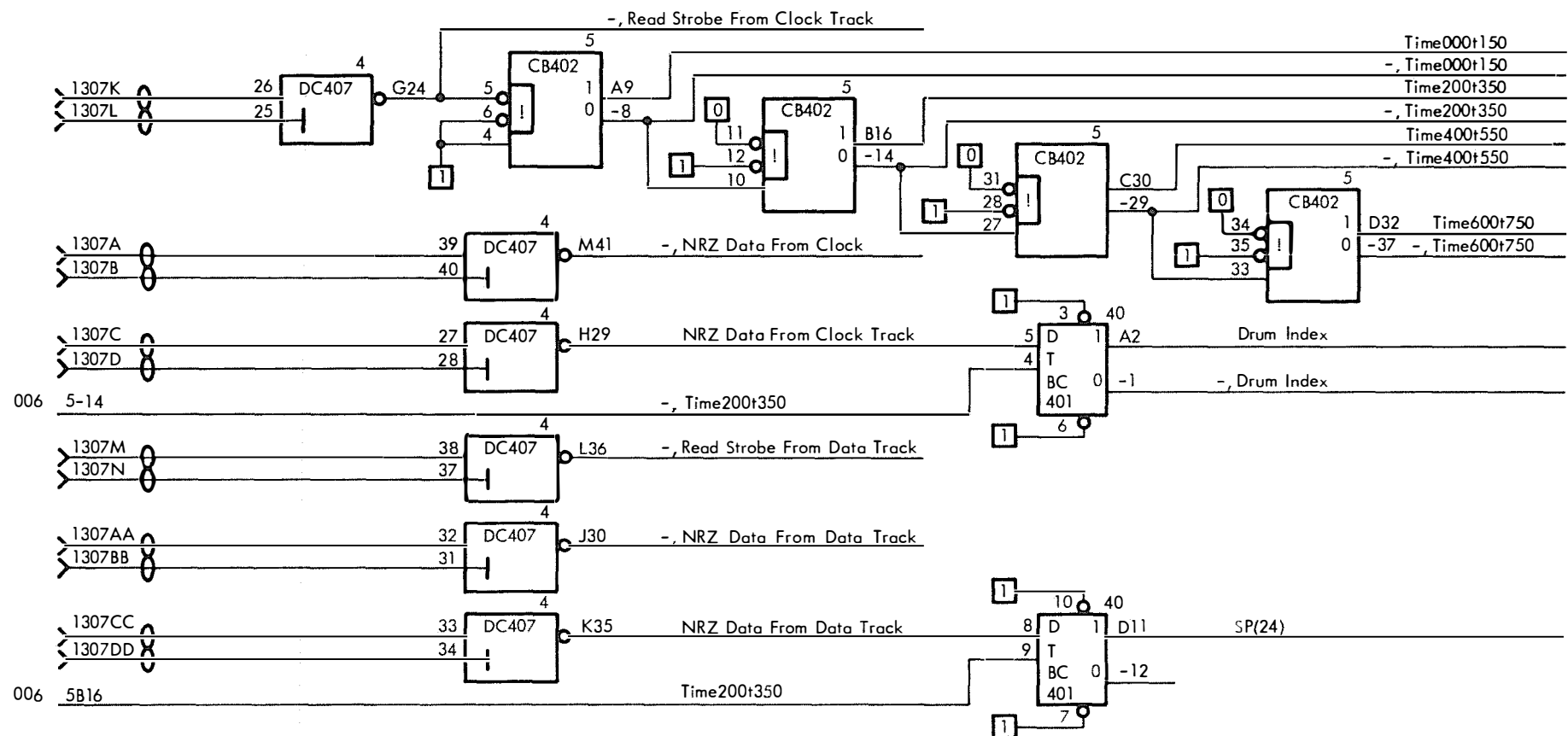
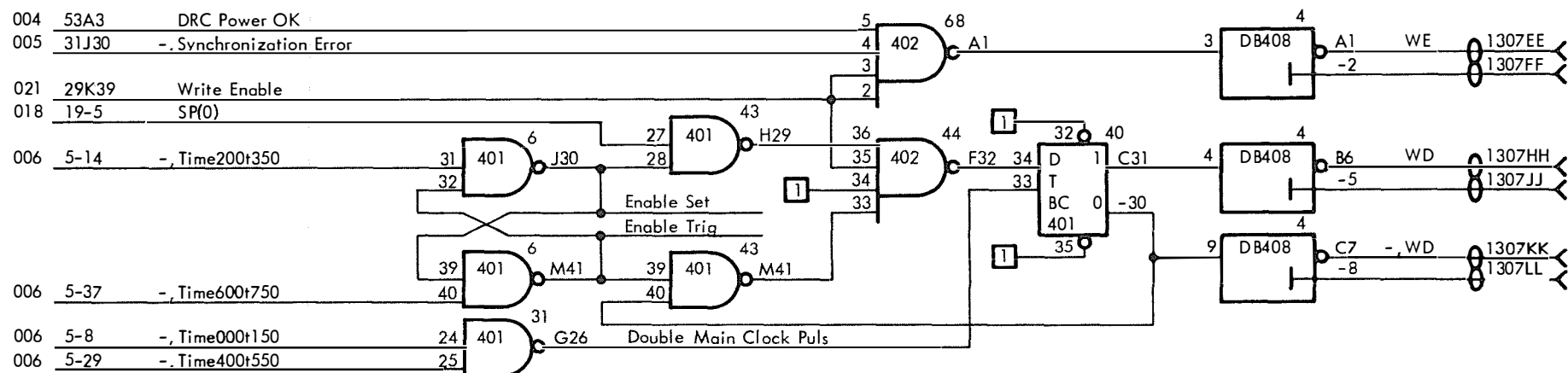
DRC032	HDC BUS(0:11)	V11479
033	HDC BUS(12:23)	V11480
034	DEVICE SELECTION, STATUS, CONNECTED, READY, AND INTERRUPT	V11481
035	IO BUS(5:16)	V11482
036	IO BUS(17:23), AND IO ENABLE, ADDRESS, ACTIVATE, AND TRANSFER	V11483
037	HDC CABLE CONNECTION	V10817
038	HDC AND LDC CABLE CONNECTIONS	V10818

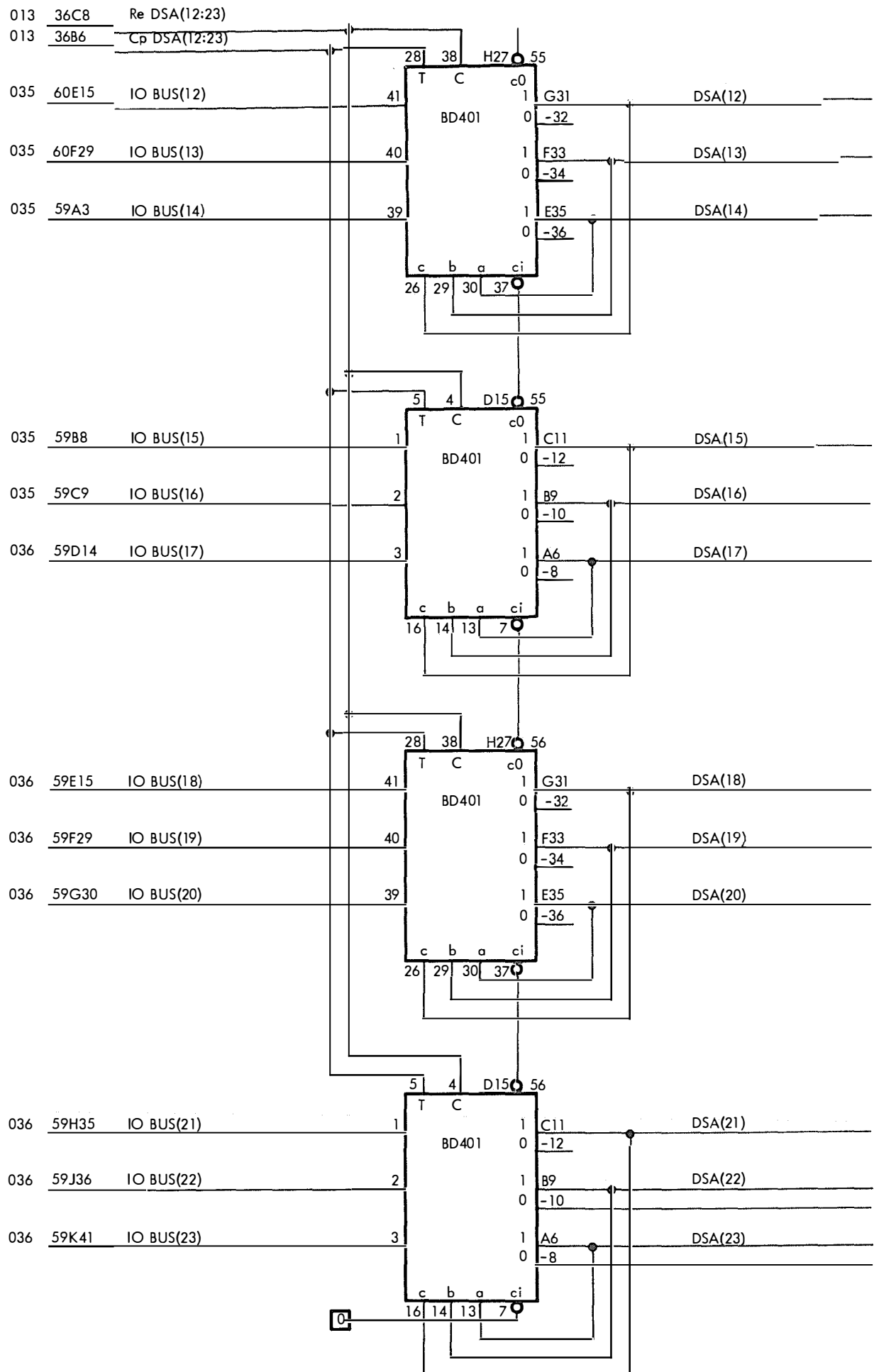


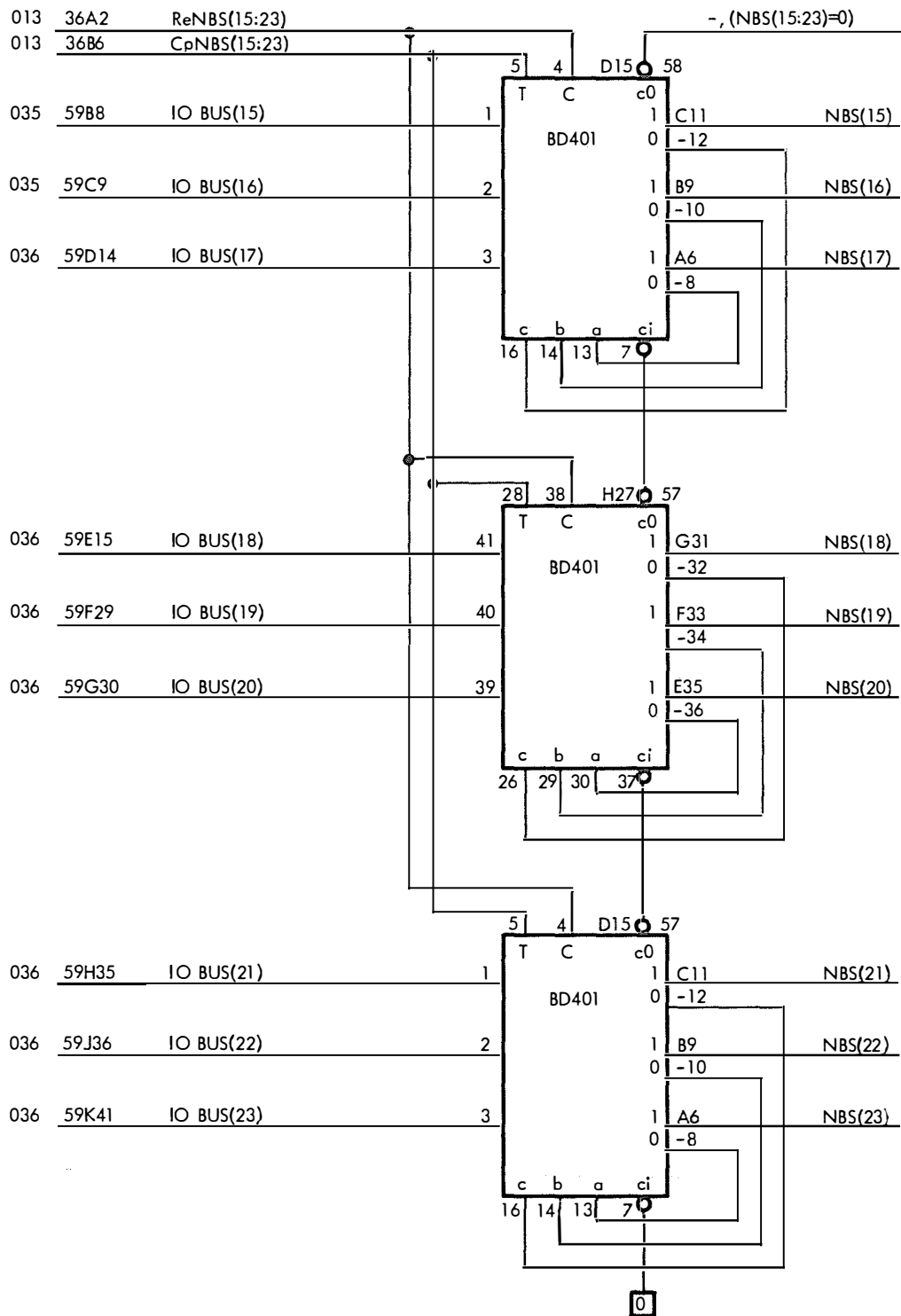


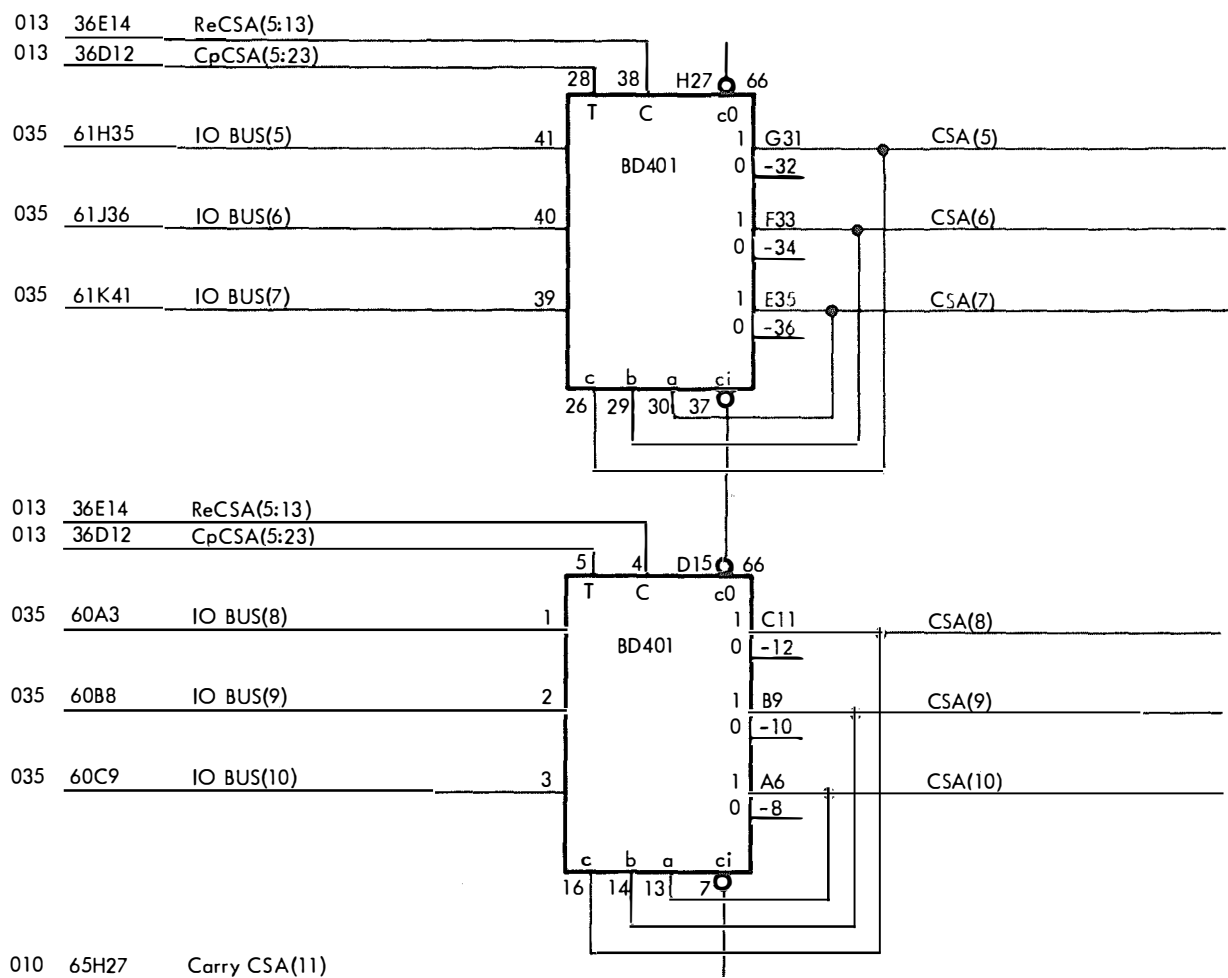




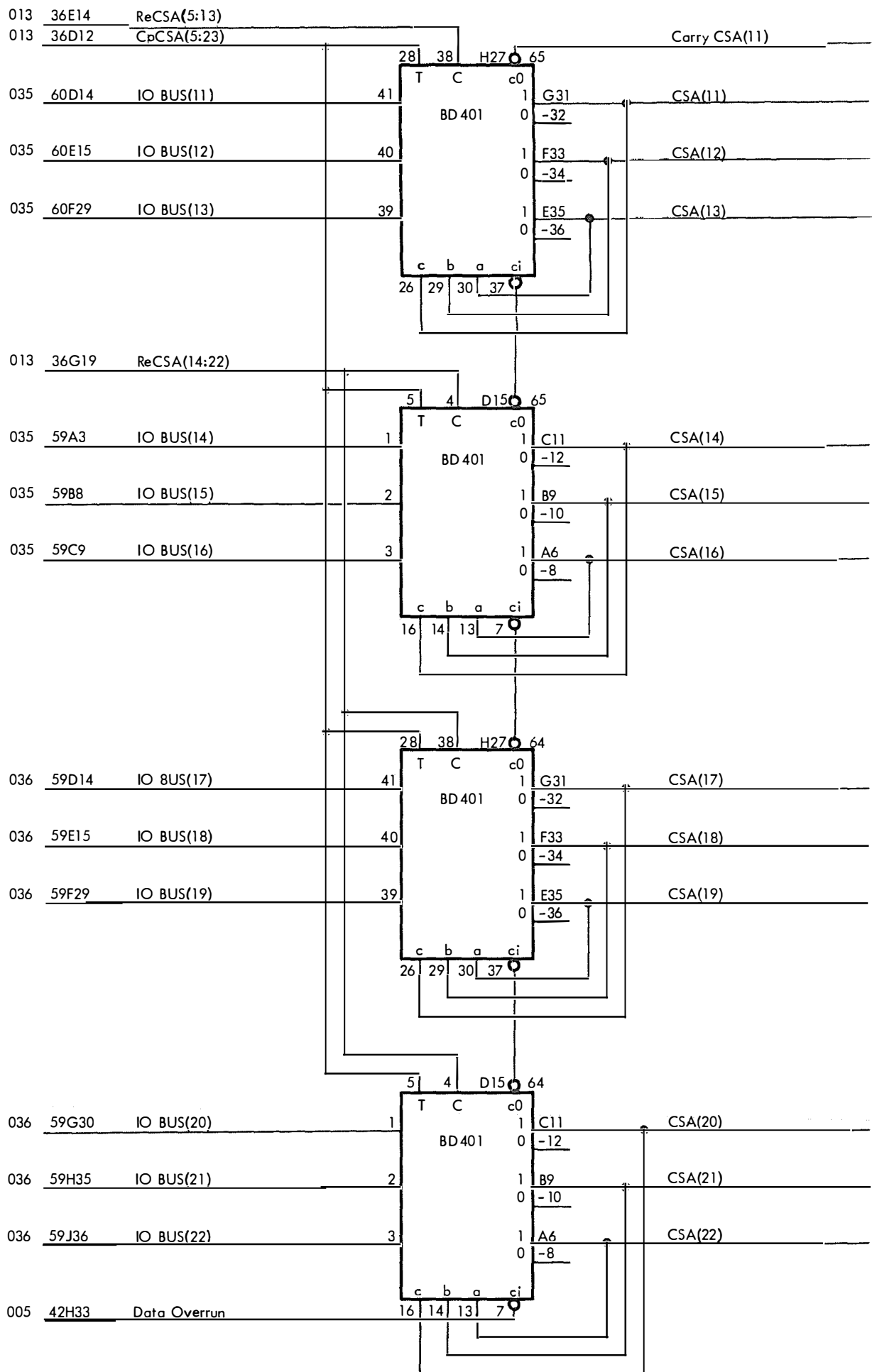


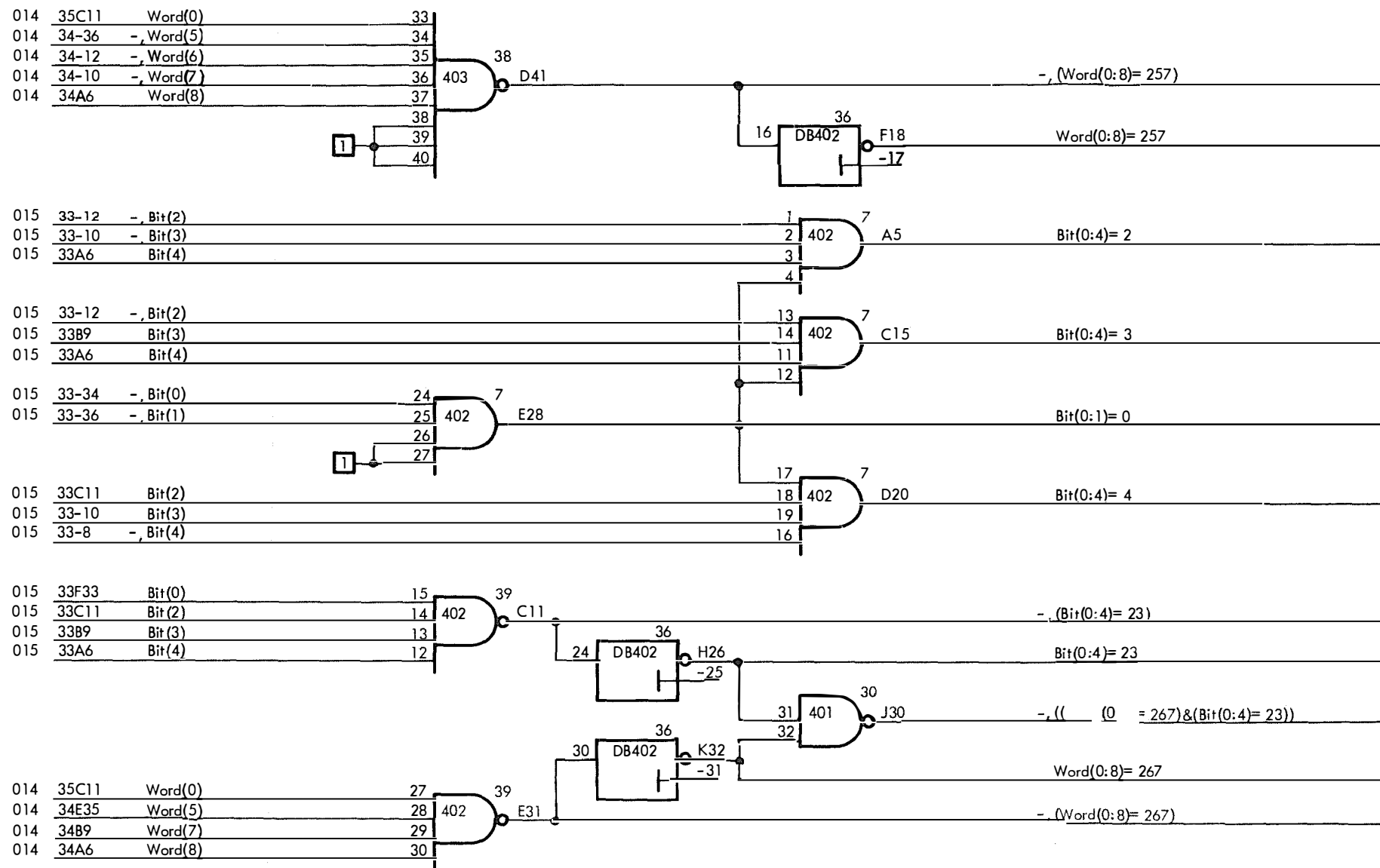


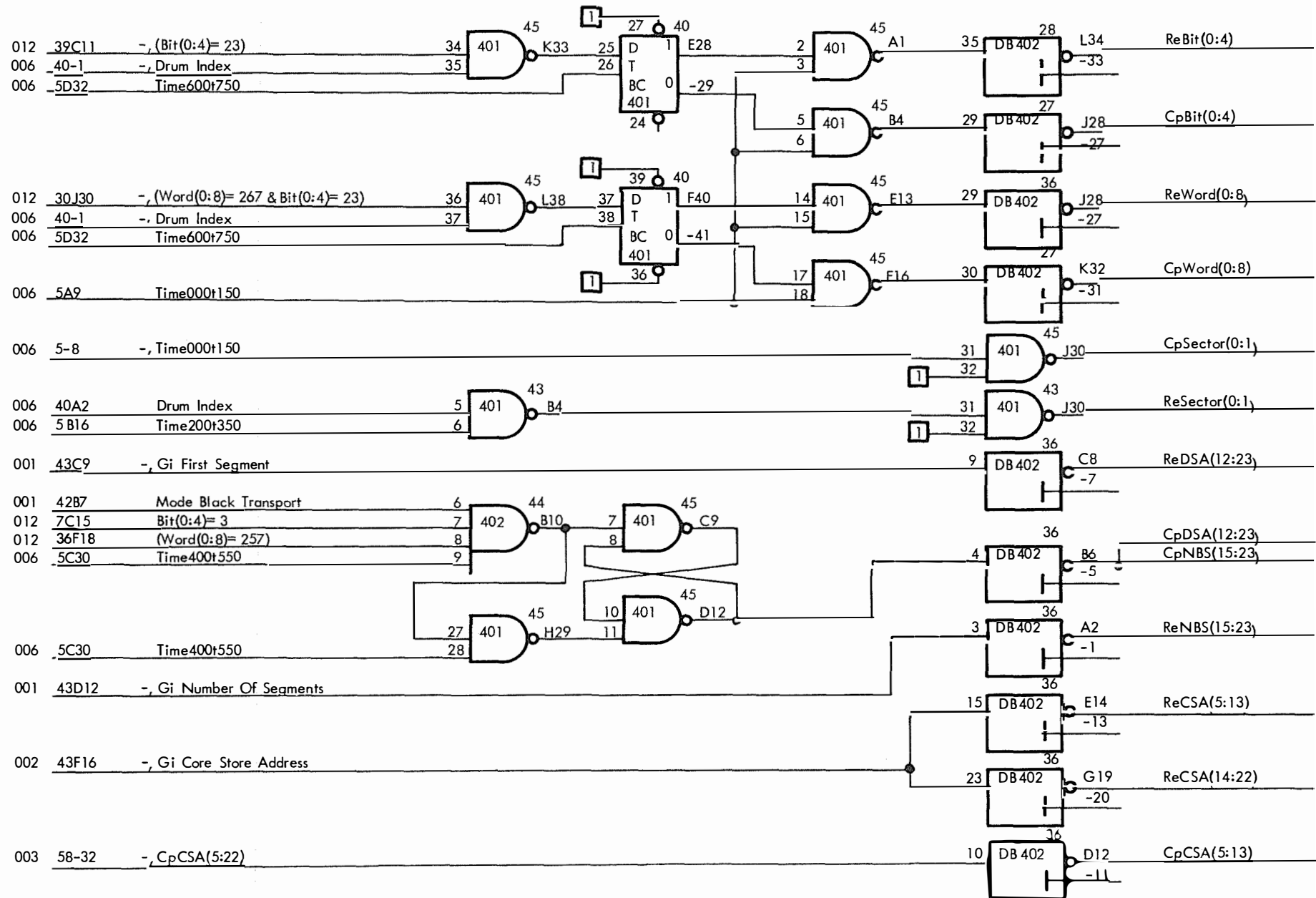


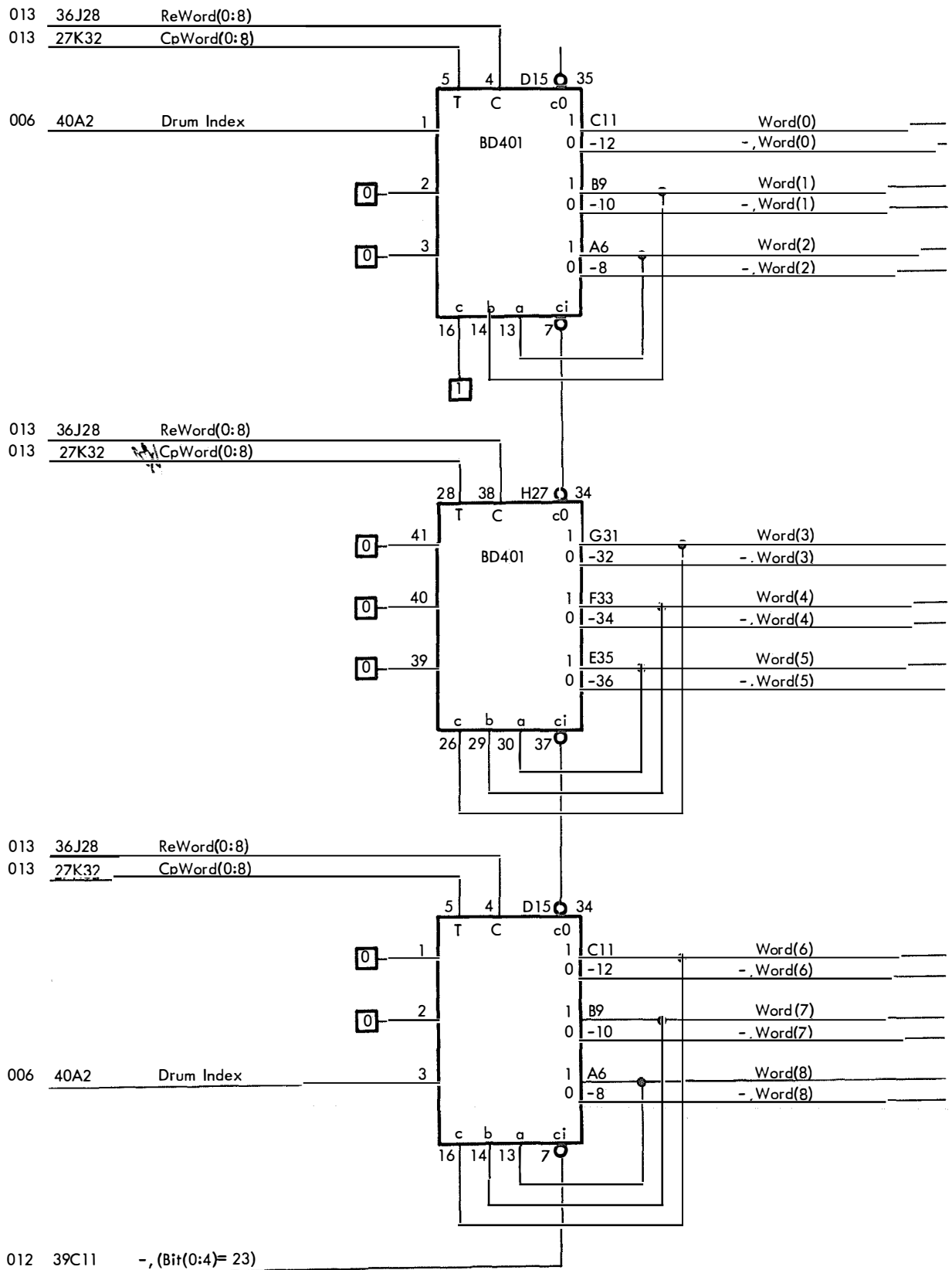


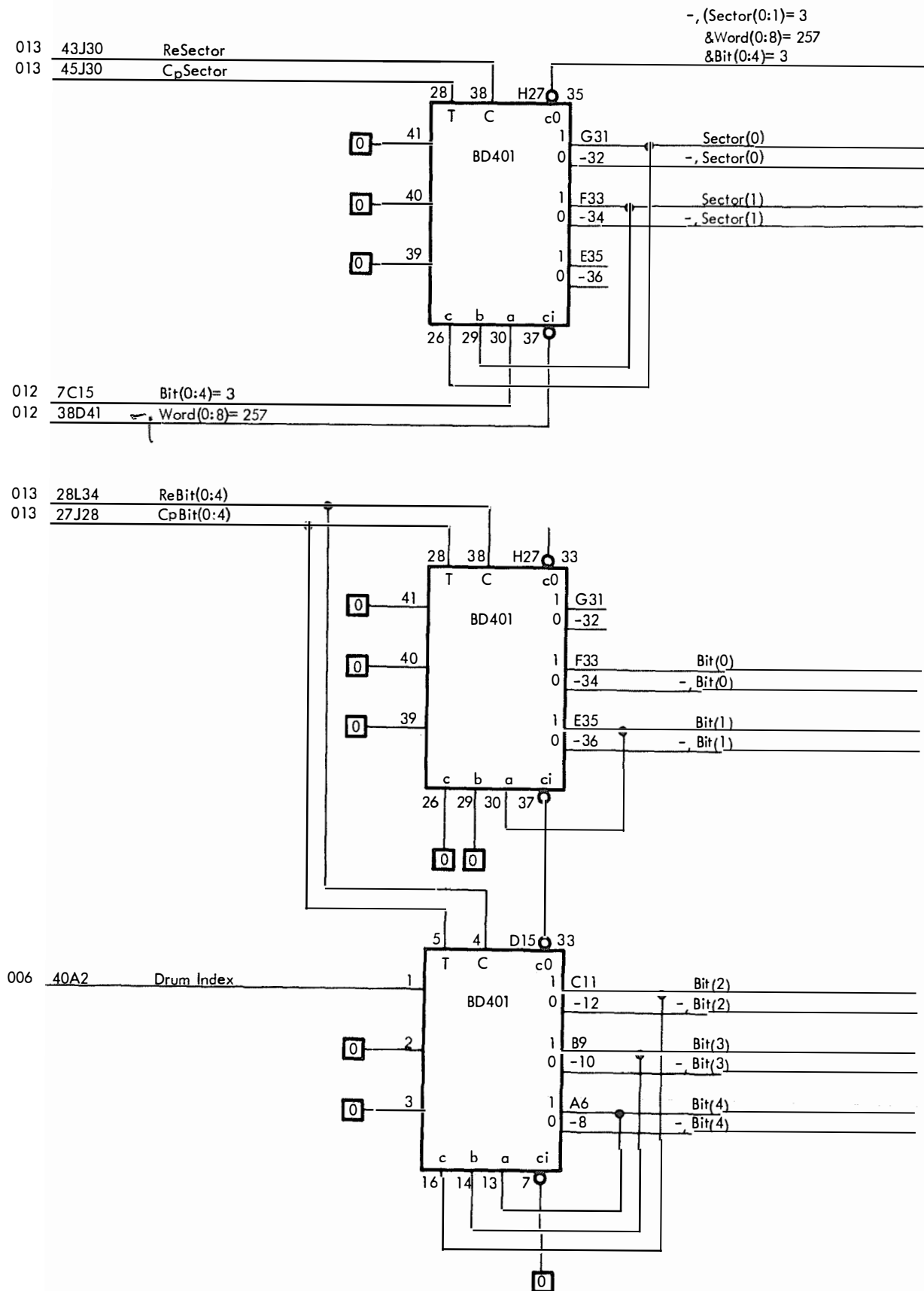
1308A	0 Volt	1308S
1308B	0 Volt	1308T
1308C	0 Volt	1308U
1308D	0 Volt	1308V
1308E	0 Volt	1308W
1308F	0 Volt	1308X
1308H	0 Volt	1308Y
1308J	0 Volt	1308Z
1308K	0 Volt	1308AA
1308L	0 Volt	1308BB
1308M	0 Volt	1308CC
1308N	0 Volt	1308DD
1308P	0 Volt	1308EE
1308R	0 Volt	1308FF

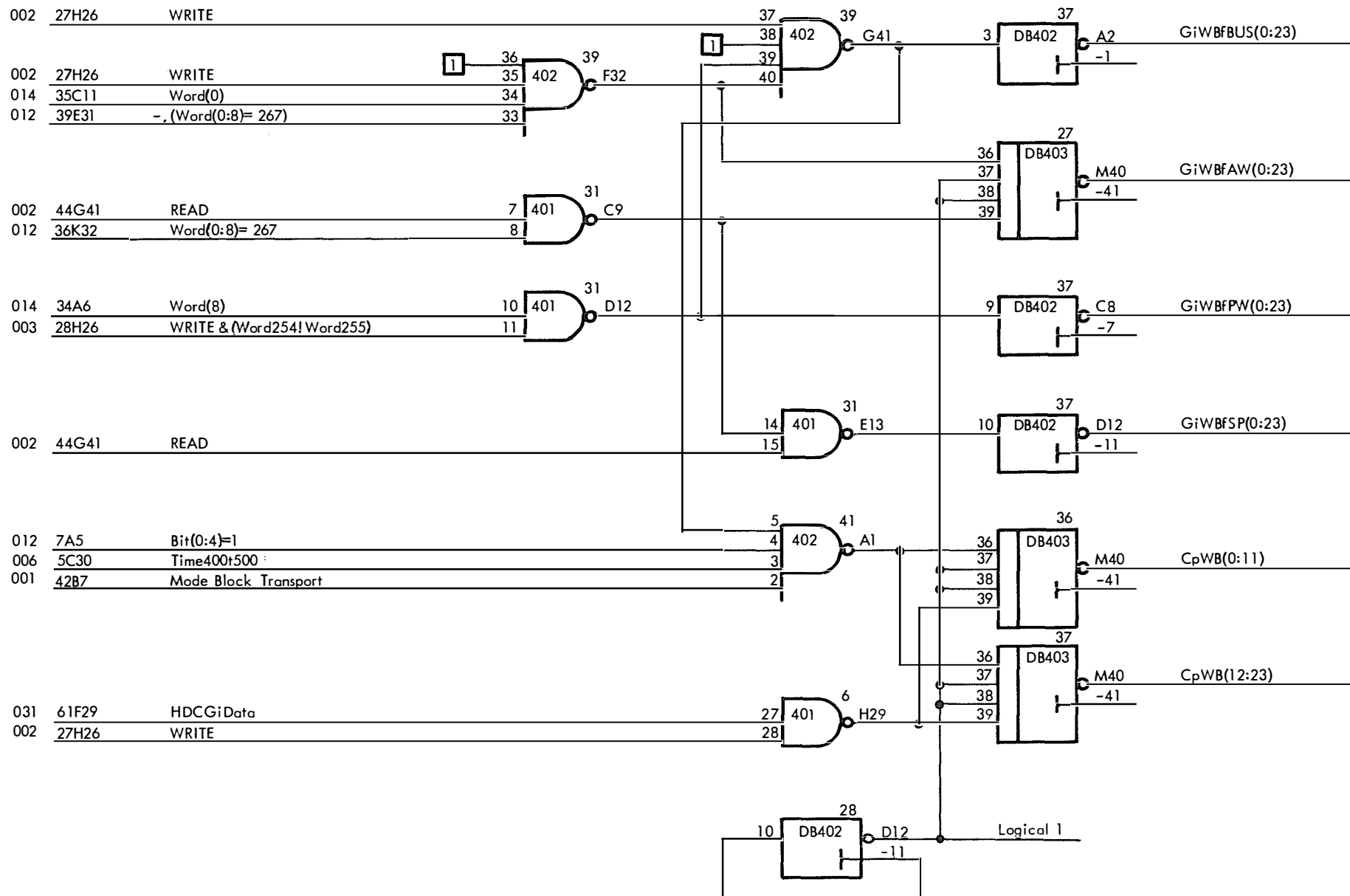


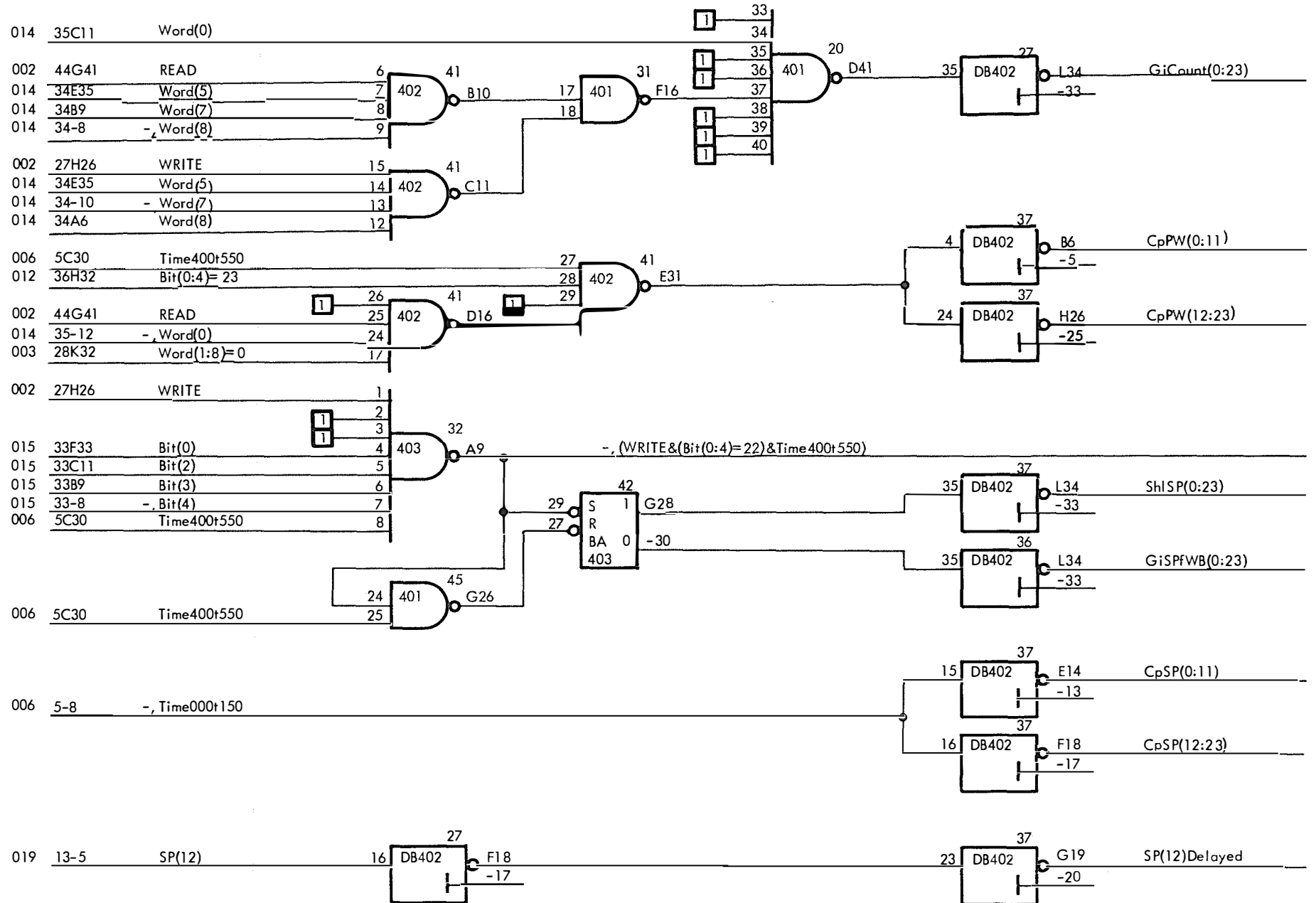


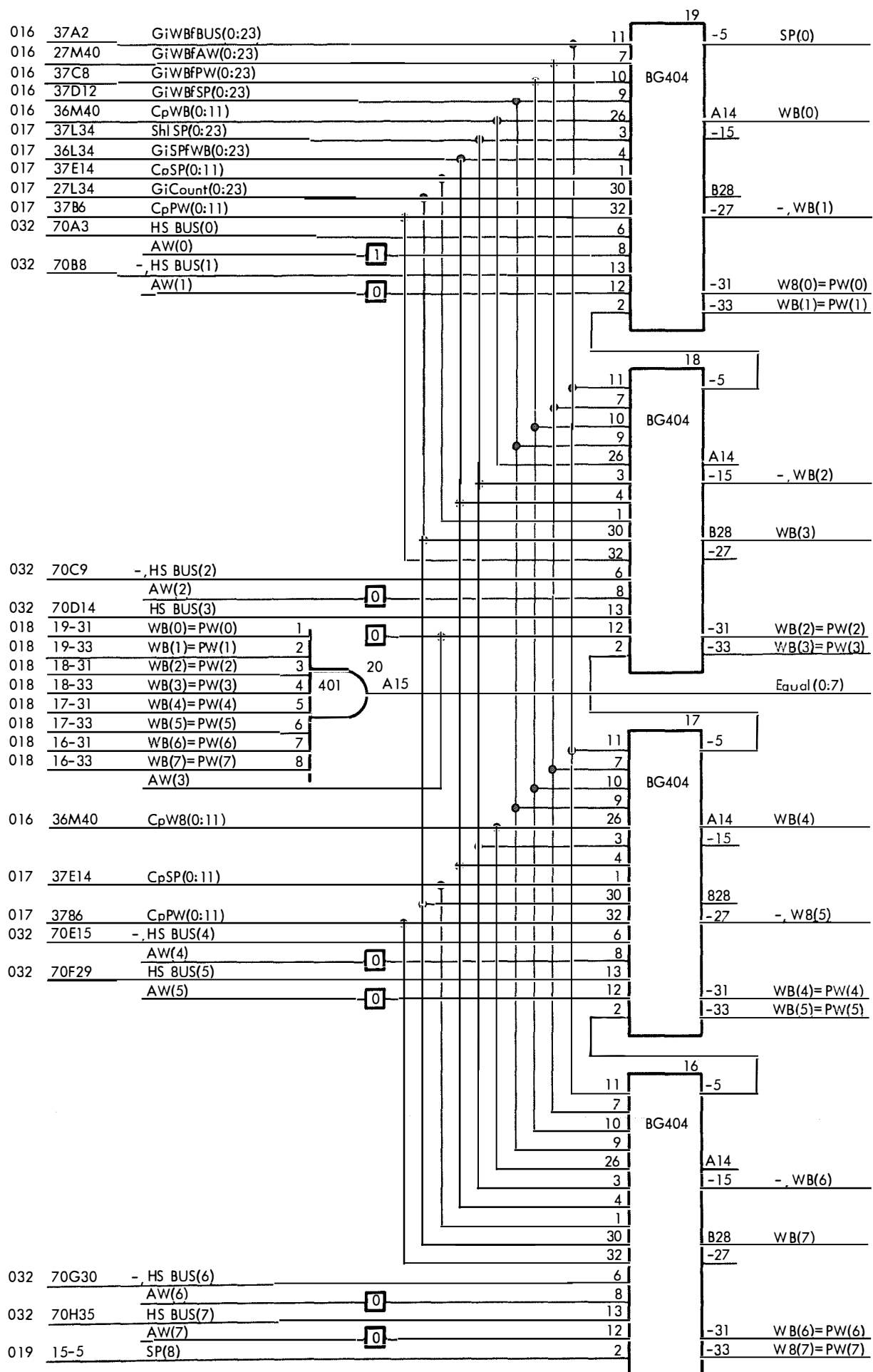


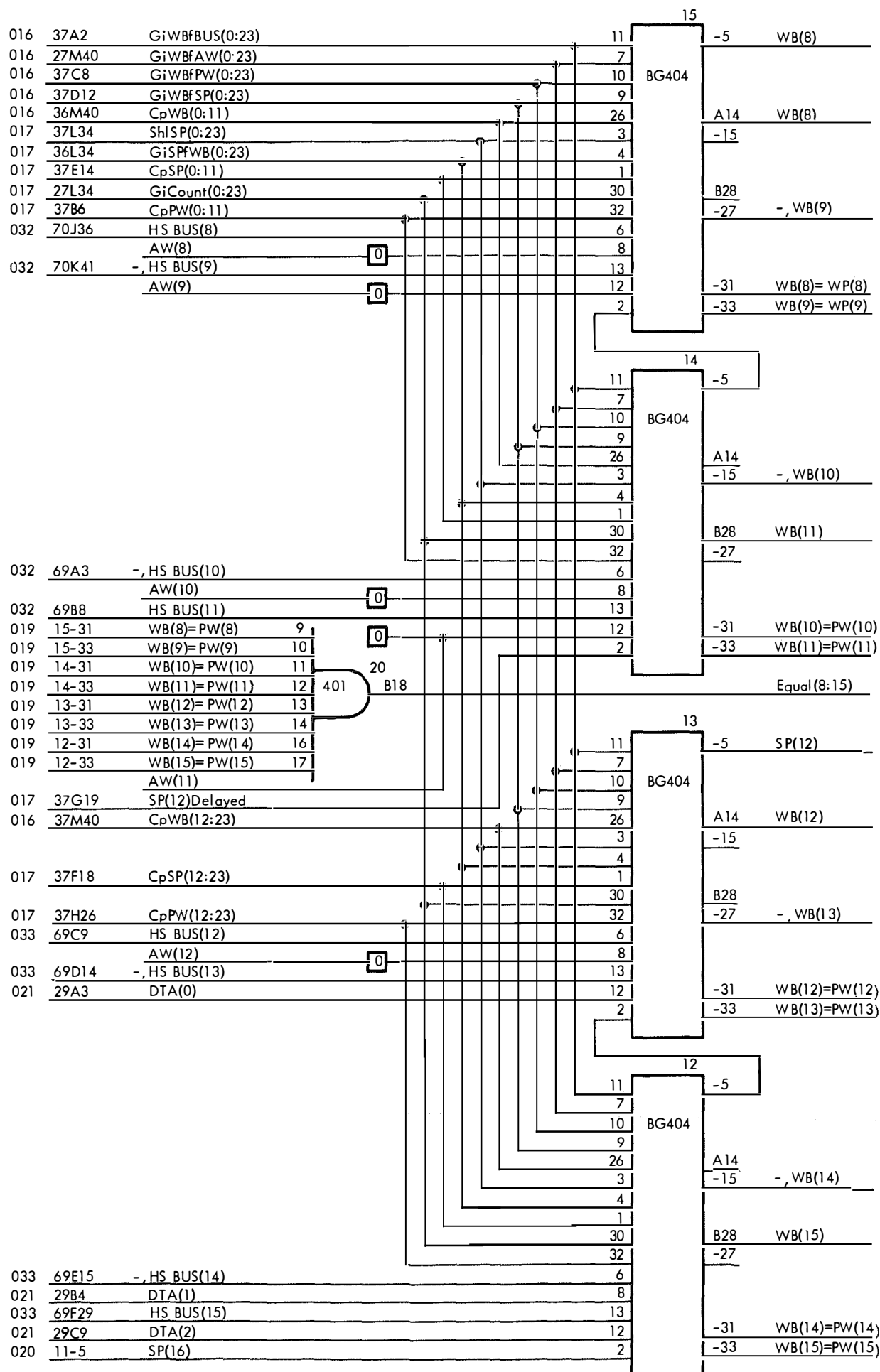


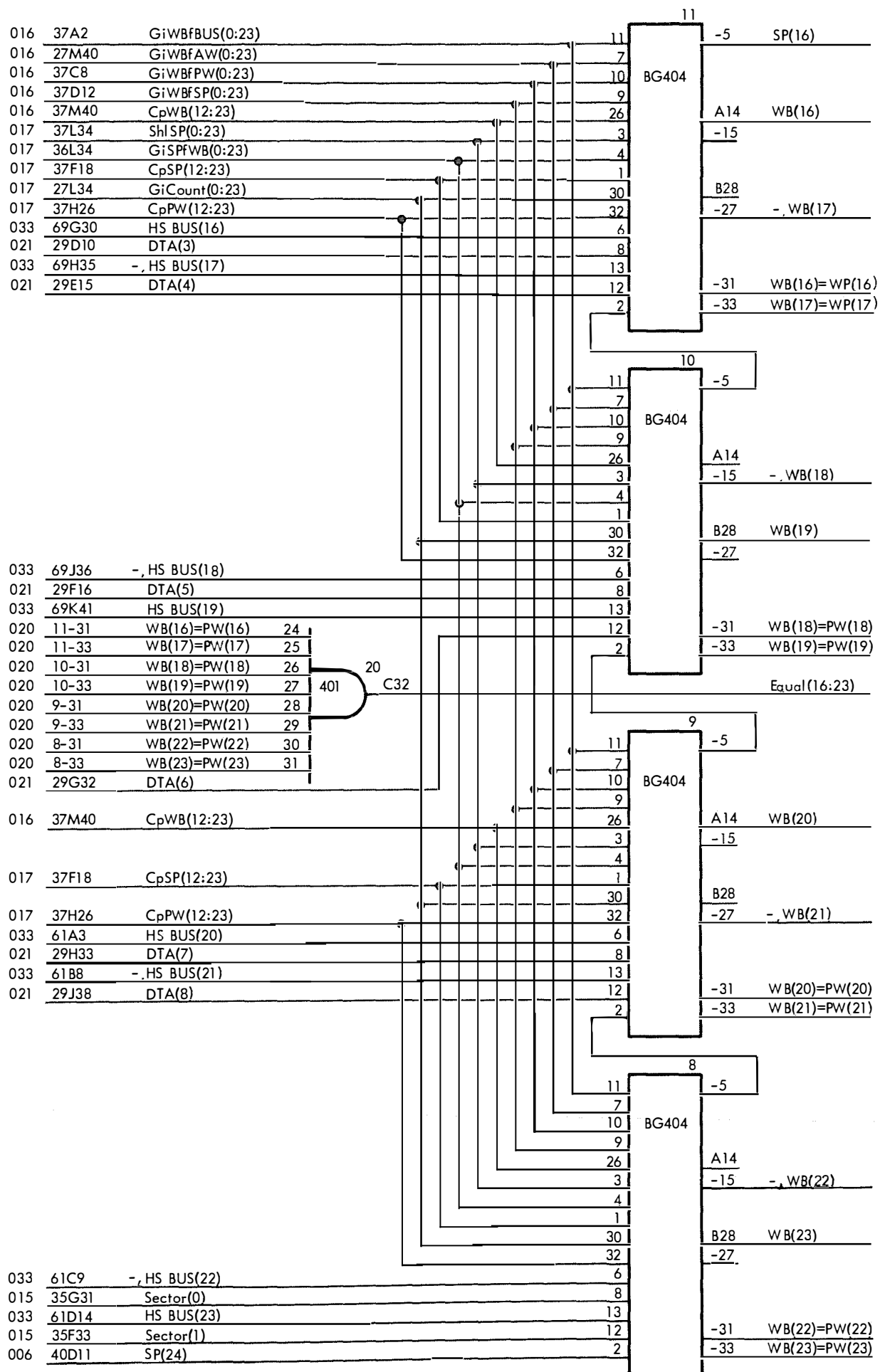


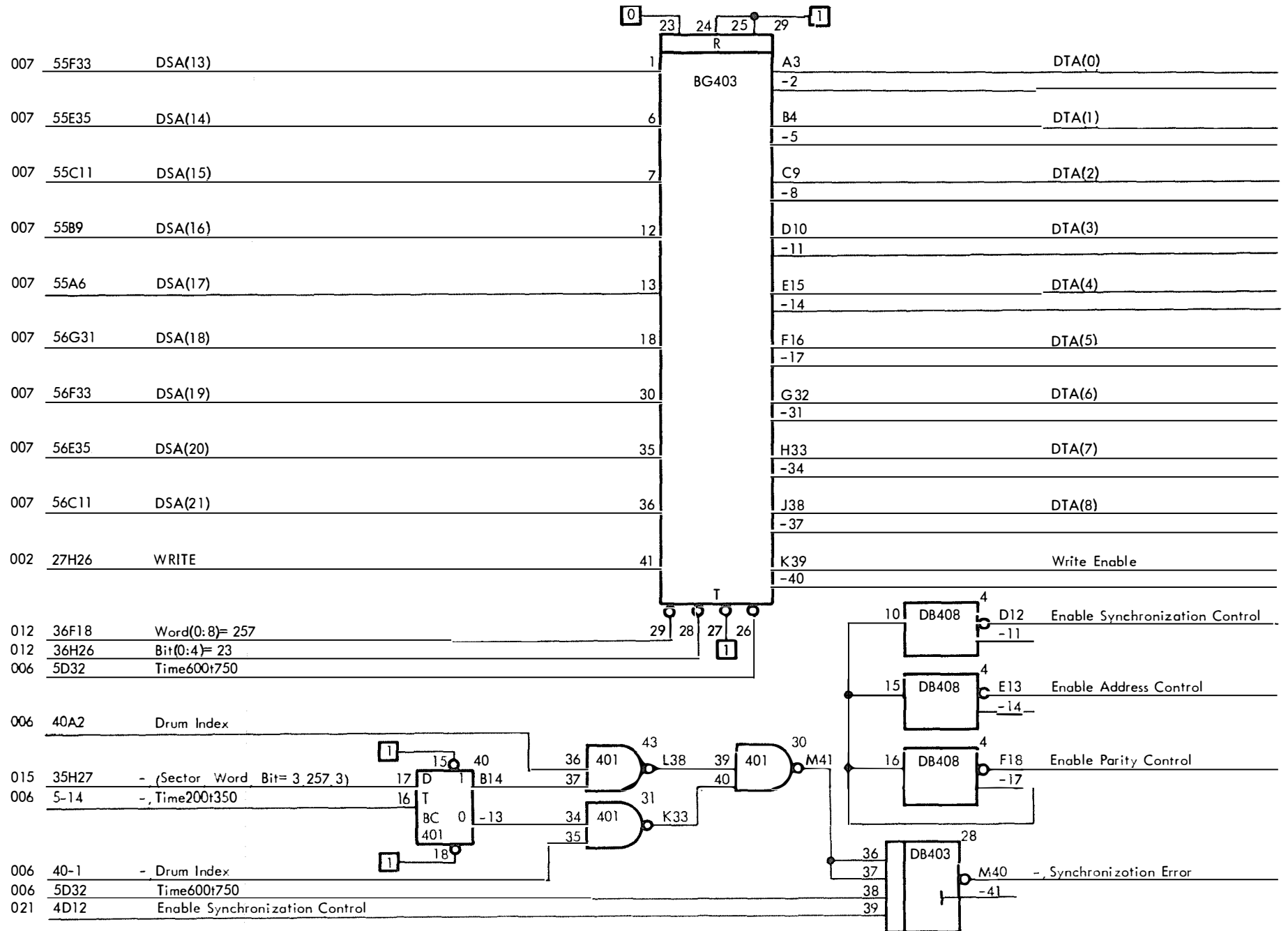


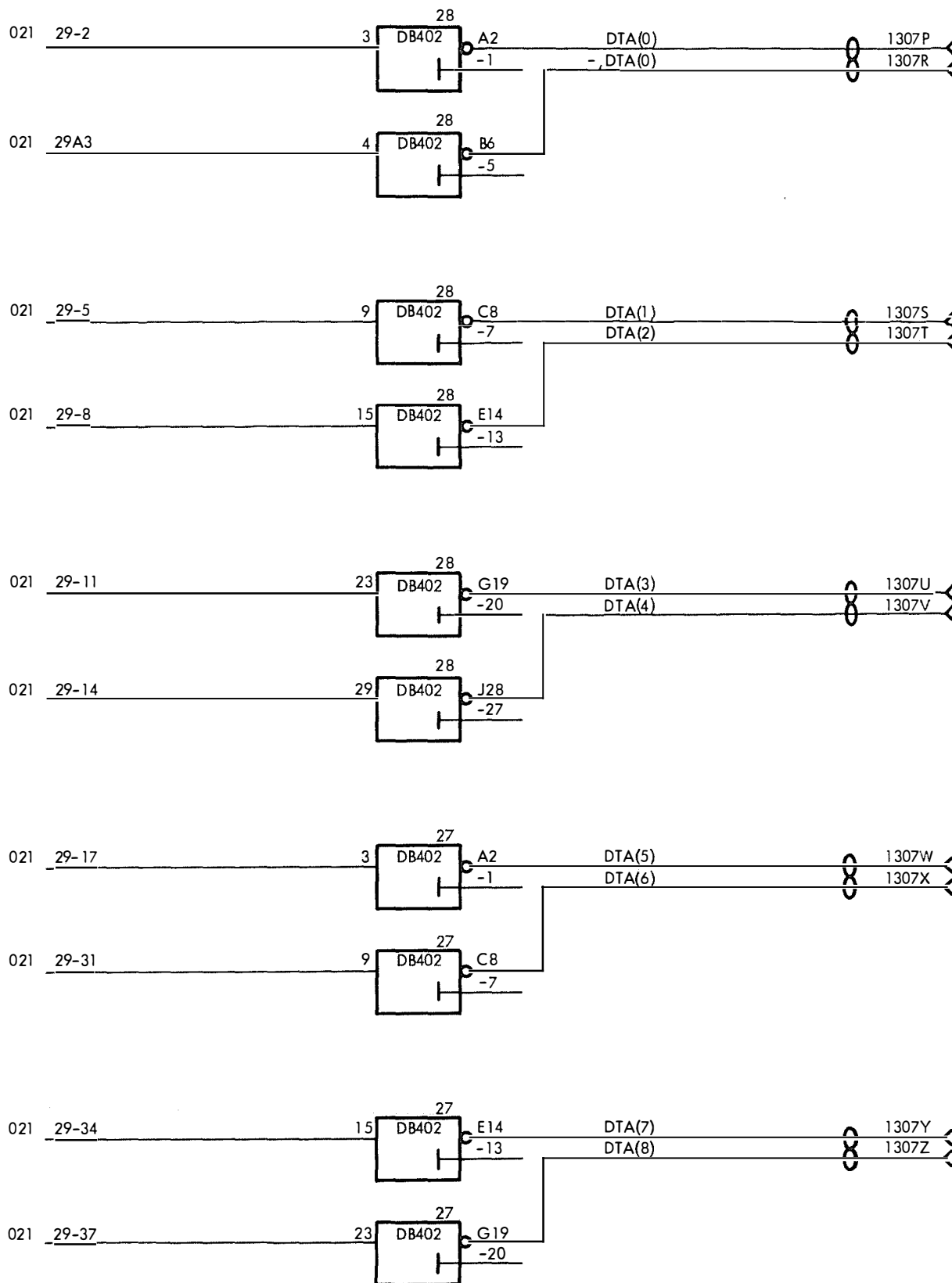


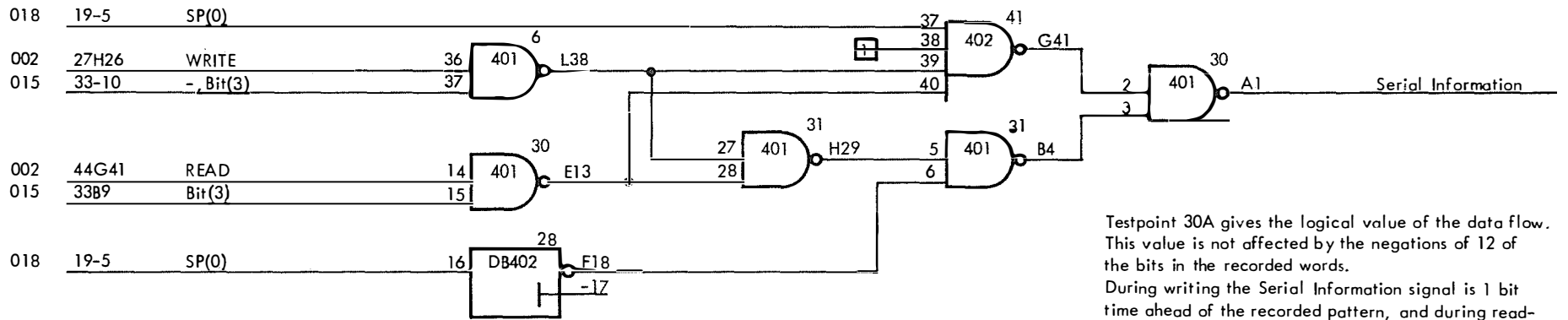












Testpoint 30A gives the logical value of the data flow. This value is not affected by the negations of 12 of the bits in the recorded words. During writing the Serial Information signal is 1 bit time ahead of the recorded pattern, and during reading, the Serial Information signal is 1 Word time plus 1 bit time delayed in comparison with the recorded pattern.

